FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-16301-1E

32-bit RISC Microcontroller

CMOS

FR30 Series MB91101

MB91101

■ DESCRIPTION

The MB91101 is a standard single-chip microcontroller constructed around the 32-bit RISC CPU (FR* family) core with abundant I/O resources and bus control functions optimized for high-performance/high-speed CPU processing for embedded controller applications. To support the vast memory space accessed by the 32-bit CPU, the MB91101 normally operates in the external bus access mode and executes instructions on the internal 1 Kbyte cache memory and 2 Kbytes RAM for enhanced performance.

The MB91101 is optimized for applications requiring high-performance CPU processing such as navigation systems, high-performance FAXs and printer controllers.

*: FR Family stands for FUJITSU RISC controller.

■ FEATURES

FR CPU

- 32-bit RISC, load/store architecture, 5-stage pipeline
- Operating clock frequency: Internal 50 MHz/external 25 MHz (PLL used at source oscillation 12.5 MHz)
- General purpose registers: 32 bits × 16
- 16-bit fixed length instructions (basic instructions), 1 instruction/1 cycle
- Memory to memory transfer, bit processing, barrel shifter processing: Optimized for embedded applications
- Function entrance/exit instructions, multiple load/store instructions of register contents, instruction systems supporting high level languages
- Register interlock functions, efficient assembly language coding
- Branch instructions with delay slots: Reduced overhead time in branch executions

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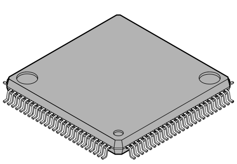
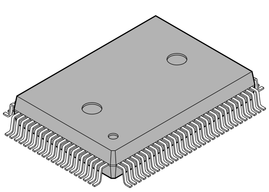
■ PACKAGE

100-pin Plastic LQFP	100-pin Plastic QFP
	
(FPT-100P-M05)	(FPT-100P-M06)

MB91101 Series

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- Internal multiplier/supported at instruction level
  Signed 32-bit multiplication: 5 cycles
  Signed 16-bit multiplication: 3 cycles
- Interrupt (push PC and PS): 6 cycles, 16 priority levels

External bus interface

- Clock doublure: Internal 50 MHz, external bus 25 MHz operation
- 25-bit address bus (32 Mbytes memory space)
- 8/16-bit data bus
- Basic external bus cycle: 2 clock cycles
- Chip select outputs for setting down to a minimum memory block size of 64 Kbytes: 6
- Interface supported for various memory technologies
  DRAM interface (area 4 and 5)
- Automatic wait cycle insertion: Flexible setting, from 0 to 7 for each area
- Unused data/address pins can be configured us input/output ports
- Little endian mode supported (Select 1 area from area 1 to 5)

DRAM interface

- 2 banks independent control (area 4 and 5)
- Normal mode (double CAS DRAM)/high-speed page mode (single CAS DRAM)/Hyper DRAM
- Basic bus cycle: Normally 5 cycles, 2-cycle access possible in high-speed page mode
- Programmable waveform: Automatic 1-cycle wait insertion to RAS and CAS cycles
- DRAM refresh
  CBR refresh (interval time configurable by 6-bit timer)
  Self-refresh mode
- Supports 8/9/10/12-bit column address width
- 2CAS/1WE, 2WE/1CAS selective

Cache memory

- 1-Kbyte instruction cache memory
- 2 way set associative
- Lock function: For specific program code to be resident in cashe memory

DMA controller (DMAC)

- 8 channels
- Transfer incident/external pins/internal resource interrupt requests
- Transfer sequence: Step transfer/block transfer/burst transfer/continuous transfer
- Transfer data length: 8 bits/16 bits/32 bits selective
- NMI/interrupt request enables temporary stop operation

UART

- 3 independent channels
- Full-duplex double buffer
- Data length: 7 bits to 9 bits (non-parity), 6 bits to 8 bits (parity)
- Asynchronous (start-stop system), CLK-synchronized communication selective
- Multi-processor mode
- Internal 16-bit timer (U-TIMER) operating as a proprietary baud rate generator: Generates any given baud rate
- Use external clock can be used as a transfer clock
- Error detection: Parity, frame, overrun

(Continued)

10-bit A/D converter (successive approximation conversion type)

- 10-bit resolution, 4 channels
- Successive approximation type: Conversion time of 5.6 µs at 25 MHz
- Internal sample and hold circuit
- Conversion mode: Single conversion/scanning conversion/repeated conversion/stop conversion selective
- Start: Software/external trigger/internal timer selective

16-bit reload timer

- 3 channels
- Internal clock: 2 clock cycle resolution, divide by 2/8/32 selective

Other interval timers

- 16-bit timer: 3 channels (U-TIMER)
- PWM timer: 4 channels
- Watchdog timer: 1 channel

Bit search module

First bit transition “1” or “0” from MSB can be detected in 1 cycle

Interrupt controller

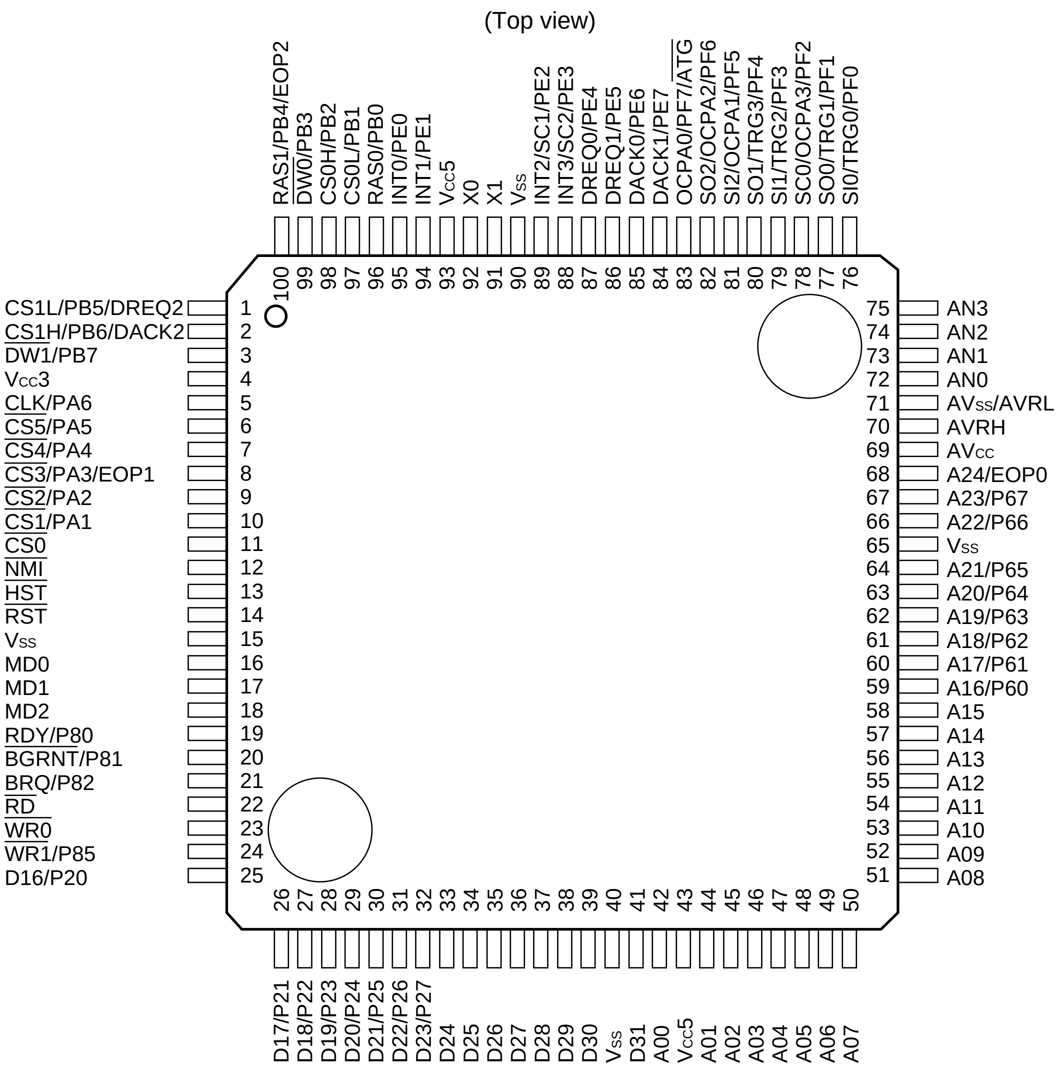
- External interrupt input: Non-maskable interrupt ($\overline{\text{NMI}}$), normal interrupt × 4 (INT0 to INT3)
- Internal interrupt incident: UART, DMA controller (DMAC), A/D converter, U-TIMER and delayed interrupt module
- Priority levels of interrupts are programmable except for non-maskable interrupt (in 16 steps)

Others

- Reset cause: Power-on reset/hardware standby/watchdog timer/software reset/external reset
- Low-power consumption mode: Sleep mode/stop mode
- Clock control
  Gear function: Operating clocks for CPU and peripherals are independently selective
  Gear clock can be selected from 1/1, 1/2, 1/4 and 1/8 (or 1/2, 1/4, 1/8 and 1/16)
  However, operating frequency for peripherals is less than 25 MHz.
- Packages: LQFP-100 and QFP-100
- CMOS technology (0.35 µm)
- Power supply voltage
  5 V: CPU power supply 5.0 V ±10% (internal regulator)
  A/D power supply 2.7 V to 3.6 V
  3 V: CPU power supply 2.7 V to 3.6 V (without internal regulator)
  A/D power supply 2.7 V to 3.6 V

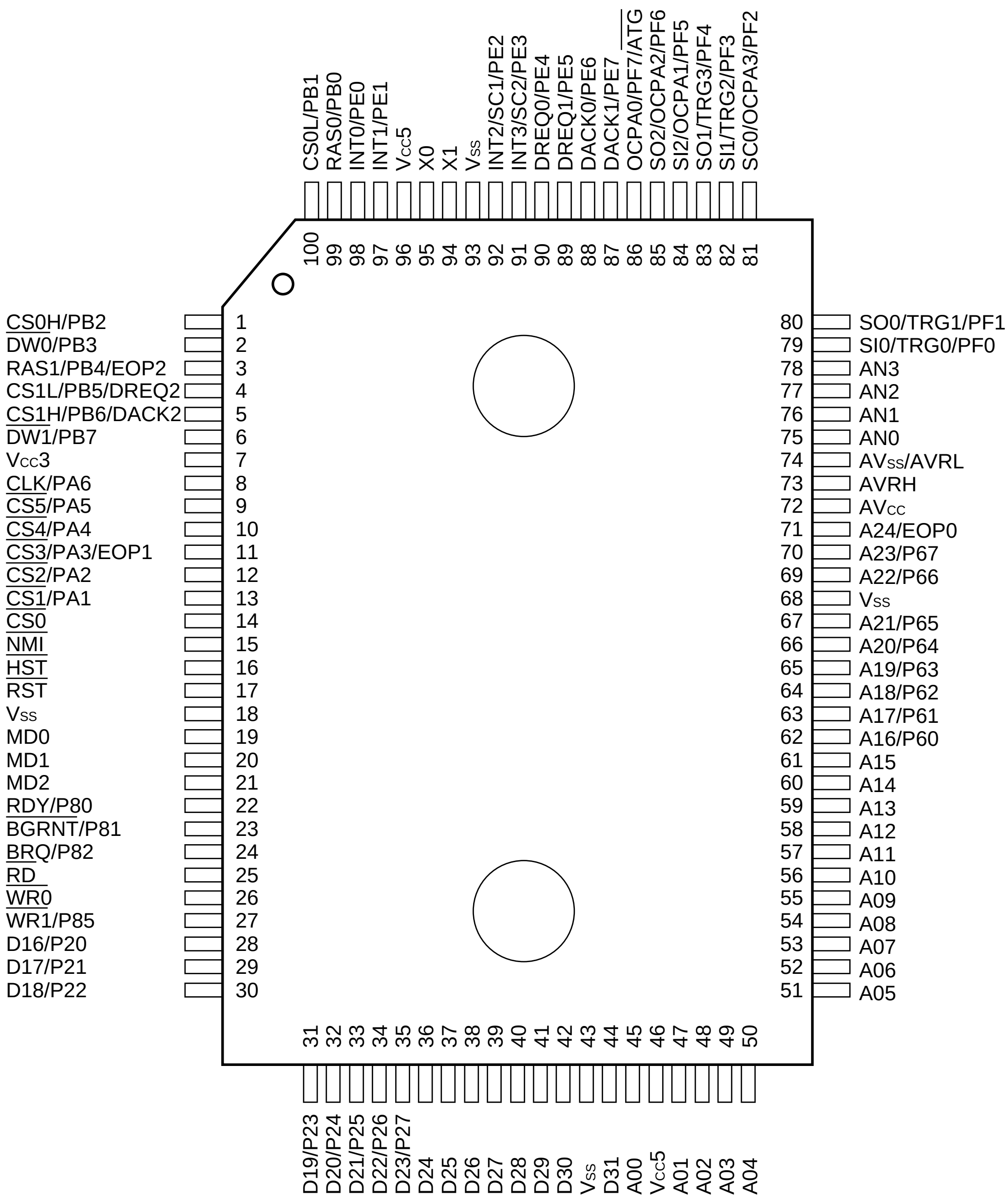
MB91101 Series

■ PIN ASSIGNMENT



(FPT-100P-M05)

(Top view)



(FPT-100P-M06)

MB91101 Series

■ PIN DESCRIPTION

Pin no. LQFP*1	Pin no. QFP*2	Pin name	Circuit type	Function
25 to 32	28 to 35	D16 to D23	C	Bit 16 to bit 23 of external data bus
		P20 to P27		Can be configured as I/O ports when external data bus width is set to 8-bit.
33 to 39, 41	36 to 42, 44	D24 to D30, D31	C	Bit 24 to bit 31 of external data bus
42, 44 to 58	45, 47 to 61	A00, A01 to A15	F	Bit 00 to bit 15 of external address bus
59 to 64, 66, 67	62 to 67, 69, 70	A16 to A21, A22, A23	F	Bit 16 to bit 23 of external address bus
		P60 to P65, P66, P67		Can be configured as I/O ports when not used as address bus.
68	71	A24	L	Bit 24 of external address bus
		EOP0		Can be configured as DMAC EOP output (ch. 0) when DMAC EOP output is enabled.
19	22	RDY	C	External ready input Inputs “0” when bus cycle is being executed and not completed.
		P80		Can be configured as a port when RDY is not used.
20	23	$\overline{BGRNT}$	F	External bus release acknowledge output Outputs “L” level when external bus is released.
		P81		Can be configured as a port when $\overline{BGRNT}$ is not used.
21	24	BRQ	C	External bus release request input Inputs “1” when release of external bus is required.
		P82		Can be configured as a port when BRQ is not used.
22	25	$\overline{RD}$	L	Read strobe output pin for external bus
23	26	$\overline{WR0}$	L	Write strobe output pin for external bus Relation between control signals and effective byte locations is as follows:

	16-bit bus width	8-bit bus width
D15 to D08	$\overline{WR0}$	$\overline{WR0}$
D07 to D00	$\overline{WR1}$	(I/O port enabled)

Note: $\overline{WR1}$ is Hi-Z during resetting.
Attach an external pull-up resister when using at 16-bit bus width.

Pin no. LQFP*1	Pin no. QFP*2	Pin name	Circuit type	Function
24	27	$\overline{WR1}$	F	(see above)
		P85		Can be configured as a port when $\overline{WR1}$ is not used.

*1: FPT-100P-M05
*2: FPT-100P-M06

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Pin no.		Pin name	Circuit type	Function
LQFP*1	QFP*2			
11	14	$\overline{CS0}$	L	Chip select 0 output (“L” active)
10	13	$\overline{CS1}$	F	Chip select 1 output (“L” active)
		PA1		Can be configured as a port when $\overline{CS1}$ is not used.
9	12	$\overline{CS2}$	F	Chip select 2 output (“L” active)
		PA2		Can be configured as a port when $\overline{CS2}$ is not used.
8	11	$\overline{CS3}$	F	Chip select 3 output (“L” active)
		PA3		Can be configured as a port when $\overline{CS3}$ and EOP1 are not used.
		EOP1		EOP output pin for DMAC (ch. 1) This function is available when EOP output for DMAC is enabled.
7	10	$\overline{CS4}$	F	Chip select 4 output (“L” active)
		PA4		Can be configured as a port when $\overline{CS4}$ is not used.
6	9	$\overline{CS5}$	F	Chip select 5 output (“L” active)
		PA5		Can be configured as a port when $\overline{CS5}$ is not used.
5	8	CLK	F	System clock output Outputs clock signal of external bus operating frequency.
		PA6		Can be configured as a port when CLK is not used.
96	99	RAS0	F	RAS output for DRAM bank 0 Refer to the DRAM interface for details.
		PB0		Can be configured as a port when RAS0 is not used.
97	100	CS0L	F	CASL output for DRAM bank 0 Refer to the DRAM interface for details.
		PB1		Can be configured as a port when CS0L is not used.
98	1	CS0H	F	CASH output for DRAM bank 0 Refer to the DRAM interface for details.
		PB2		Can be configured as a port when CS0H is not used.
99	2	$\overline{DW0}$	F	$\overline{WE}$ output for DRAM bank 0 (“L” active) Refer to the DRAM interface for details.
		PB3		Can be configured as a port when $\overline{DW0}$ is not used.
100	3	RAS1	F	RAS output for DRAM bank 1 Refer to the DRAM interface for details.
		PB4		Can be configured as a port when RAS1 and EOP2 are not used.
		EOP2		DMAC EOP output (ch. 2) This function is available when DMAC EOP output is enabled.

*1: FPT-100P-M05
*2: FPT-100P-M06

(Continued)

MB91101 Series

Pin no.		Pin name	Circuit type	Function
LQFP*1	QFP*2			
1	4	CS1L	F	CASL output for DRAM bank 1 Refer to the DRAM interface for details.
		PB5		Can be configured as a port when CS1L and DREQ are not used.
		DREQ2		External transfer request input pin for DMA This pin is used for input when external trigger is selected to cause DMAC operation, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
2	5	CS1H	F	CASH output for DRAM bank 1 Refer to the DRAM interface for details.
		PB6		Can be configured as a port when CS1H and DACK2 are not used.
		DACK2		External transfer request acknowledge output pin for DMAC (ch. 2) This function is available when transfer request output for DMAC is enabled.
3	6	$\overline{\text{DW1}}$	F	$\overline{\text{WE}}$ output for DRAM bank 1 (“L” active) Refer to the DRAM interface for details.
		PB7		Can be configured as a port when $\overline{\text{DW1}}$ is not used.
16 to 18	19 to 21	MD0 to MD2	G	Mode pins 0 to 2 MCU basic operation mode is set by these pins. Directly connect these pins with V_{CC} or V_{SS} for use.
92	95	X0	A	Clock (oscillator) input
91	94	X1	A	Clock (oscillator) output
14	17	$\overline{\text{RST}}$	B	External reset input
13	16	$\overline{\text{HST}}$	H	Hardware standby input (“L” active)
12	15	$\overline{\text{NMI}}$	H	NMI (non-maskable interrupt pin) input (“L” active)
95, 94	98, 97	INT0, INT1	F	External interrupt request input pins These pins are used for input during corresponding interrupt is enabled, and it is necessary to disable output for other functions from these pins unless such output is made intentionally.
		PE0, PE1		Can be configured as a port when INT0, INT1 are not used.
89	92	INT2	F	External interrupt request input pin This pin is used for input during corresponding interrupt is enabled, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
		SC1		Clock I/O pin for UART1 Clock output is available when clock output of UART1 is enabled.
		PE2		Can be configured as a port when INT2 and SC1 are not used. This function is available when UART1 clock output is disabled.

*1: FPT-100P-M05
*2: FPT-100P-M06

(Continued)

Pin no.		Pin name	Circuit type	Function
LQFP*1	QFP*2			
88	91	INT3	F	External interrupt request input pin This pin is used for input during corresponding interrupt is enabled, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
		SC2		UART2 clock I/O pin Clock output is available when UART2 clock output is enabled.
		PE3		Can be configured as a port when INT3 and SC2 are not used. This function is available when UART2 clock output is disabled.
87, 86	90, 89	DREQ0, DREQ1	F	External transfer request input pins for DMA These pins are used for input when external trigger is selected to cause DMAC operation, and it is necessary to disable output for other functions from these pins unless such output is made intentionally.
		PE4, PE5		Can be configured as a port when DREQ0, DREQ1 are not used.
85	88	DACK0	F	External transfer request acknowledge output pin for DMAC (ch. 0) This function is available when transfer request output for DMAC is enabled.
		PE6		Can be configured as a port when DACK0 is not used. This function is available when transfer request acknowledge output for DMAC or DACK0 output is disabled.
84	87	DACK1	F	External transfer request acknowledge output pin for DMAC (ch. 1) This function is available when transfer request output for DMAC is enabled.
		PE7		Can be configured as a port when DACK1 is not used. This function is available when transfer request output for DMAC or DACK1 output is disabled.
76	79	SI0	F	UART0 data input pin This pin is used for input during UART0 is in input operation, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
		TRG0		PWM timer external trigger input pin This pin is used for input during PWM timer external trigger is in input operation, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
		PF0		Can be configured as a port when SI0 and TRG0 are not used.

*1: FPT-100P-M05
*2: FPT-100P-M06

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MB91101 Series

Pin no.		Pin name	Circuit type	Function
LQFP*1	QFP*2			
77	80	SO0	F	UART0 data output pin This function is available when UART0 data output is enabled.
		TRG1		PWM timer external trigger input pin This function is available when serial data output of PF1, UART0 are disabled.
		PF1		Can be configured as a port when SO0 and TRG1 are not used. This function is available when serial data output of UART0 is disabled.
78	81	SC0	F	UART0 clock I/O pin Clock output is available when UART0 clock output is enabled.
		OCPA3		PWM timer output pin This function is available when PWM timer output is enabled.
		PF2		Can be configured as a port when SC0 and OCPA3 are not used. This function is available when UART0 clock output is disabled.
79	82	SI1	F	UART1 data input pin This pin is used for input during UART1 is in input operation, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
		TRG2		PWM timer external trigger input pin This pin is used for input during PWM timer external trigger is in input operation, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
		PF3		Can be configured as a port when SI1 and TRG2 are not used.
80	83	SO1	F	UART1 data output pin This function is available when UART1 data output is enabled.
		TRG3		PWM timer external trigger input pin This function is available when PF4, UART1 data outputs are disabled.
		PF4		Can be configured as a port when SO1 and TRG3 are not used. This function is available when UART1 data output is disabled.
81	84	SI2	F	UART2 data input pin This pin is used for input during UART2 is in input operation, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
		OCPA1		PWM timer output pin This function is available when PWM timer output is enabled.
		PF5		Can be configured as a port when SI2 and OCPA2 are not used.

*1: FPT-100P-M05
*2: FPT-100P-M06

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Pin no.		Pin name	Circuit type	Function
LQFP*1	QFP*2			
82	85	SO2	F	UART2 data output pin This function is available when UART2 data output is enabled.
		OCPA2		PWM timer output pin This function is available when PWM timer output is enabled.
		PF6		Can be configured as a port when SO2 and OCPA2 are not used. This function is available when UART2 data output is disabled.
83	86	OCPA0	F	PWM timer output pin This function is available when PWM timer output is enabled.
		PF7		Can be configured as a port when OCPA0 and $\overline{ATG}$ are not used. This function is available when PWM timer output is disabled.
		$\overline{ATG}$		External trigger input pin for A/D converter This pin is used for input when external trigger is selected to cause A/D converter operation, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
72 to 75	75 to 78	AN0 to AN3	D	Analog input pins of A/D converter This function is available when AIC register is set to specify analog input mode.
69	72	AV_{CC}	—	Power supply pin (V_{CC}) for A/D converter
70	73	AVRH	—	Reference voltage input (high) for A/D converter Make sure to turn on and off this pin with potential of AVRH or more applied to V_{CC}.
71	74	AV_{SS}, AVRL	—	Power supply pin (V_{SS}) for A/D converter and reference voltage input pin (low)
43, 93	46, 96	$V_{CC}5$	—	5 V power supply pin (V_{CC}) for digital circuit Always two pins must be connected to the power supply (connect to 3 V power supply when operating at 3 V).
4	7	$V_{CC}3$	—	Bypass capacitor pin for internal capacitor. Also connect this pin to 3 V power supply when operating at 3 V.
15, 40, 65, 90	18, 43, 68, 93	V_{SS}	—	Earth level (V_{SS}) for digital circuit

*1: FPT-100P-M05
*2: FPT-100P-M06

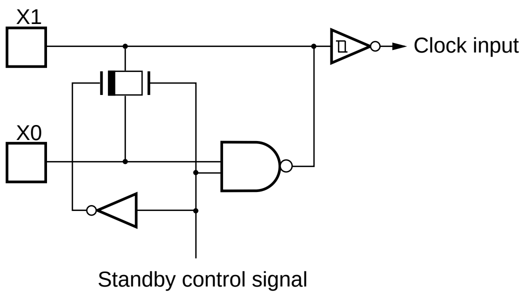
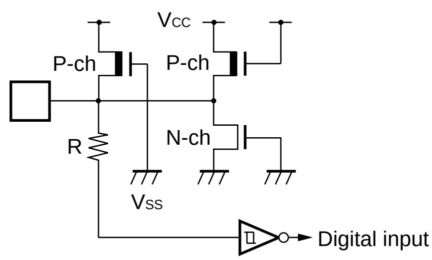
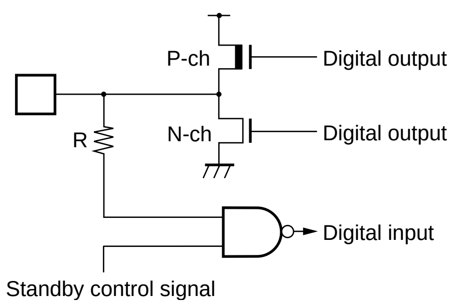
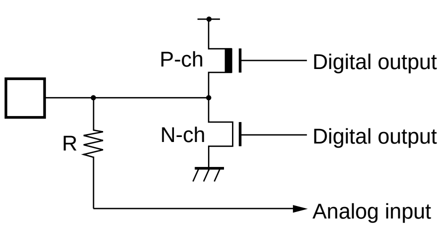
Note: In most of the above pins, I/O port and resource I/O are multiplexed e.g. P82 and BRQ. In case of conflict between output of I/O port and resource I/O, priority is always given to the output of resource I/O.

MB91101 Series

■ DRAM CONTROL PIN

Pin name	Data bus 16-bit mode		Data bus 8-bit mode	Remarks
	2CAS/1WR mode	1CAS/2WR mode	—	
RAS0	Area 4 RAS	Area 4 RAS	Area 4 RAS	Correspondence of “L” “H” to lower address 1 bit (A0) in data bus 16-bit mode “L”: “0” “H”: “1” CASL: CAS which A0 corresponds to “0” area CASH: CAS which A0 corresponds to “1” area $\overline{\text{WEL}}$: $\overline{\text{WE}}$ which A0 corresponds to “0” area $\overline{\text{WEH}}$: $\overline{\text{WE}}$ which A0 corresponds to “1” area
RAS1	Area 5 RAS	Area 5 RAS	Area 5 RAS	
CS0L	Area 4 CASL	Area 4 CAS	Area 4 CAS	
CS0H	Area 4 CASH	Area 4 $\overline{\text{WEL}}$	Area 4 CAS	
CS1L	Area 5 CASL	Area 5 CAS	Area 5 CAS	
CS1H	Area 5 CASH	Area 5 $\overline{\text{WEL}}$	Area 5 CAS	
$\overline{\text{DW0}}$	Area 4 $\overline{\text{WE}}$	Area 4 $\overline{\text{WEH}}$	Area 4 $\overline{\text{WE}}$	
$\overline{\text{DW1}}$	Area 5 $\overline{\text{WE}}$	Area 5 $\overline{\text{WEH}}$	Area 5 $\overline{\text{WE}}$	

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		• Oscillation feedback resistance 1 MΩ approx. With standby control
B		• CMOS level Hysteresis input Without standby control With pull-up resistance
C		• CMOS level I/O With standby control
D		• Analog input

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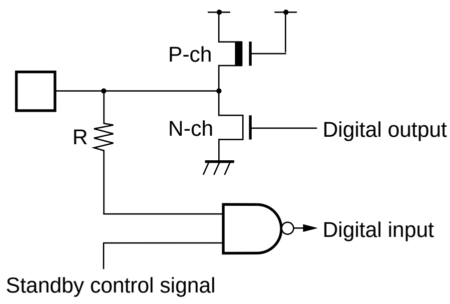
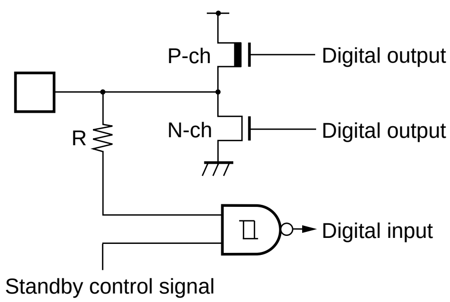
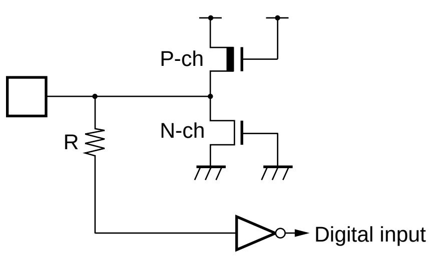
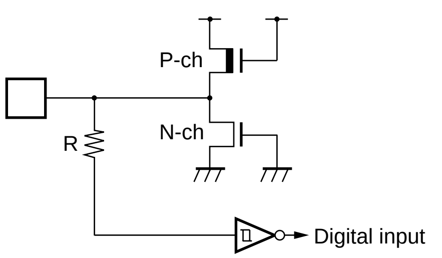
Type	Circuit	Remarks
E		• N-ch open-drain output • CMOS level input With standby control
F		• CMOS level output • CMOS level Hysteresis input With standby control
G		• CMOS level input Without standby control
H		• CMOS level Hysteresis input Without standby control

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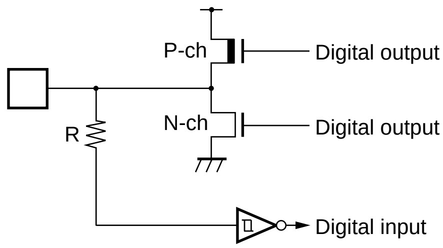
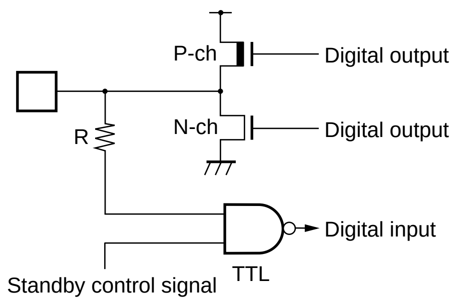
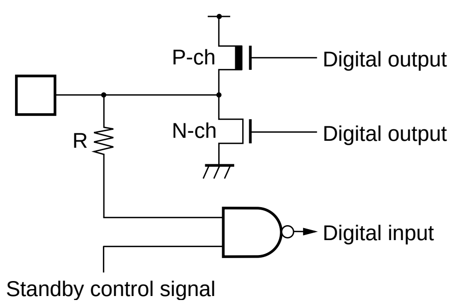
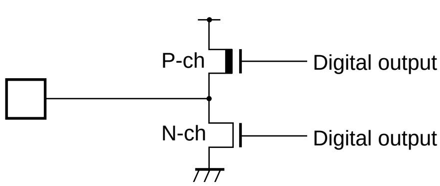
Type	Circuit	Remarks
I		• CMOS level output • CMOS level Hysteresis input Without standby control
J		• CMOS level output • TTL level input With standby control
K		• CMOS level input/output With standby control • Large current drive
L		• CMOS level output

MB91101 Series

■ HANDLING DEVICES

1. Preventing Latchup

In CMOS ICs, applying voltage higher than V_{CC} or lower than V_{SS} to input/output pin or applying voltage over rating across V_{CC} and V_{SS} may cause latchup.

This phenomenon rapidly increases the power supply current, which may result in thermal breakdown of the device. Make sure to prevent the voltage from exceeding the maximum rating.

Take care that the analog power supply (AV_{CC} AVR) and the analog input do not exceed the digital power supply (V_{CC}) when the analog power supply turned on or off.

2. Treatment of Unused Pins

Unused pins left open may cause malfunctions. Make sure to connect them to pull-up or pull-down resistors.

3. External Reset Input

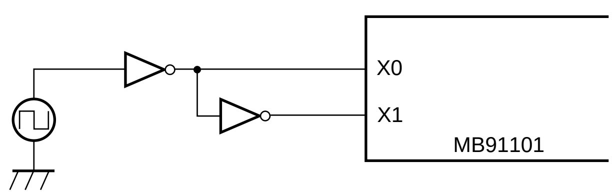
It takes at least 5 machine cycle to input “L” level to the $\overline{\text{RST}}$ pin and to ensure inner reset operation properly.

4. Remarks for External Clock Operation

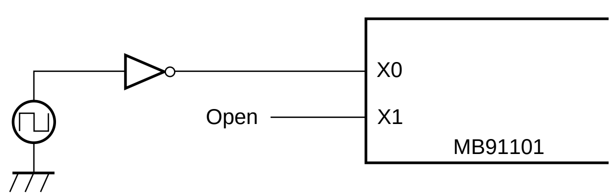
When external clock is selected, supply it to X0 pin generally, and simultaneously the opposite phase clock to X0 must be supplied to X1 pin. However, in this case the stop mode must not be used (because X1 pin stops at “H” output in stop mode).

And can be used to supply only to X0 pin with 5 V power supply at 12.5 MHz and less than.

- **Using an external clock**



Using an external clock (normal)
Note: Can not be used stop mode (oscillation stop mode).



Using an external clock (can be used at 12.5 MHz and less than.)
(5 V power supply only)

5. Power Supply Pins

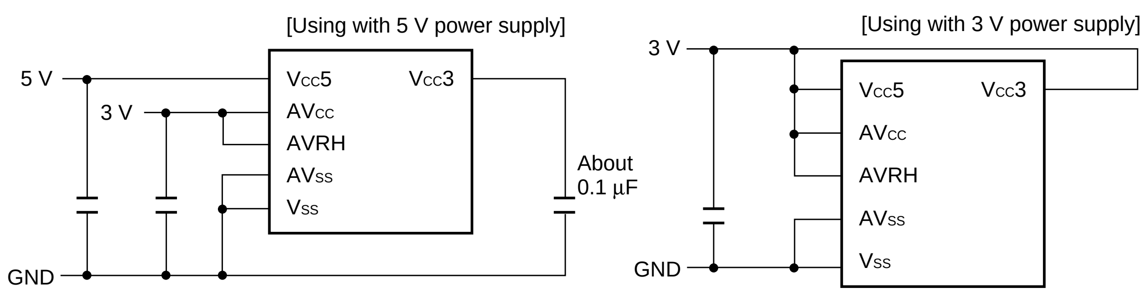
When there are several V_{CC} and V_{SS} pins, each of them is equipotentially connected to its counterpart inside of the device, minimizing the risk of malfunctions such as latch up. To further reduce the risk of malfunctions, to prevent EMI radiation, to prevent strobe signal malfunction resulting from creeping-up of ground level and to observe the total output current standard, connect all V_{CC} and V_{SS} pins to the power supply or GND.

It is preferred to connect V_{CC} and V_{SS} of MB91101 to power supply with minimal impedance possible.

It is also recommended to connect a ceramic capacitor as a bypass capacitor of about 0.1 µF between V_{CC} and V_{SS} at a position as close as possible to MB91101.

MB91101 has an internal regulator. When using with 5 V power supply, supply 5 V to $V_{CC}5$ pin and make sure to connect about 0.1 µF bypass capacitor to $V_{CC}3$ pin for regulator. And another 3 V power supply is needed for the A/D convertor. When using with 3 V power supply, connect both $V_{CC}5$ pin and $V_{CC}3$ pin to the 3 V power supply.

• **Connecting to a power supply**



6. Crystal Oscillator Circuit

Noises around X0 and X1 pins may cause malfunctions of MB91101. In designing the PC board, layout X0, X1 and crystal oscillator (or ceramic oscillator) and bypass capacitor for grounding as close as possible.

It is strongly recommended to design PC board so that X1 and X0 pins are surrounded by grounding area for stable operation.

7. Turning-on Sequence of A/D Converter Power Supply and Analog Input

Make sure to turn on the digital power supply (V_{CC}) before turning on the A/D converter (AV_{CC}, AVRH) and applying voltage to analog input (AN0 to AN3).

Make sure to turn off digital power supply after power supply to A/D converters and analog inputs have been switched off. (There are no such limitations in turning on power supplies. Analog and digital power supplies may be turned on simultaneously.) Make sure that AVRH never exceeds AV_{CC} when turning on/off power supplies.

8. Treatment of N.C. Pins

Make sure to leave N.C. pins open.

MB91101 Series

9. Fluctuation of Power Supply Voltage

Warranty range for normal operation against fluctuation of power supply voltage V_{CC} is as given in rating. However, sudden fluctuation of power supply voltage within the warranty range may cause malfunctions. It is recommended to make every effort to stabilize the power supply voltage to IC. It is also recommended that by controlling power supply as a reference of stabilizing, V_{CC} ripple fluctuation (P-P value) at the commercial frequency (50 Hz to 60 Hz) should be less than 10% of the standard V_{CC} value and the transient regulation should be less than 0.1 V/ms at instantaneous deviation like turning off the power supply.

10. Mode Setting Pins (MD0 to MD2)

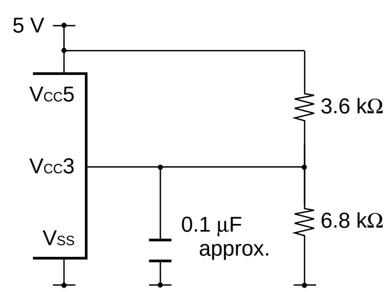
Connect mode setting pins (MD0 to MD2) directly to V_{CC} or V_{SS}.

Arrange each mode setting pin and V_{CC} or V_{SS} patterns on the printed circuit board as close as possible and make the impedance between them minimal to prevent mistaken entrance to the test mode caused by noises.

11. Internal DC Regulator

Internal DC regulator stops in stop mode. When the regulator stops owing to the increase of inner leakage current (ICCH) in stop mode, malfunction caused by noise or any troubles about power supply in normal operation, the internal 3 V power supply voltage may decrease less than the warranty range for normal operation. So when using the internal regulator and stop mode with 5 V power supply, never fail to support externally so that 3 V power supply voltage might not decrease. However, even in such a case, the internal regulator can be restarted by inputting the reset procedure. (In this case, set the reset to “L” level within the oscillation stabilizing waiting time.)

- **Using STOP mode with 5 V power supply**



12. Turning on the Power Supply

When turning on the power supply, never fail to start from setting the $\overline{RST}$ pin to “L” level. And after the power supply voltage goes to V_{CC} level, at least after ensuring the time for 5 machine cycle, then set to “H” level.

13. Pin Condition at Turning on the Power Supply

The pin condition at turning on the power supply is unstable. The circuit starts being initialized after turning on the power supply and then starting oscillation and then the operation of the internal regulator becomes stable. So it takes about 42 ms for the pin to be initialized from the oscillation starting at the source oscillation 12.5 MHz. Take care that the pin condition may be output condition at initial unstable condition.

14. Source Oscillation Input at Turning on the Power Supply

At turning on the power supply, never fail to input the clock before cancellation of the oscillation stabilizing waiting.

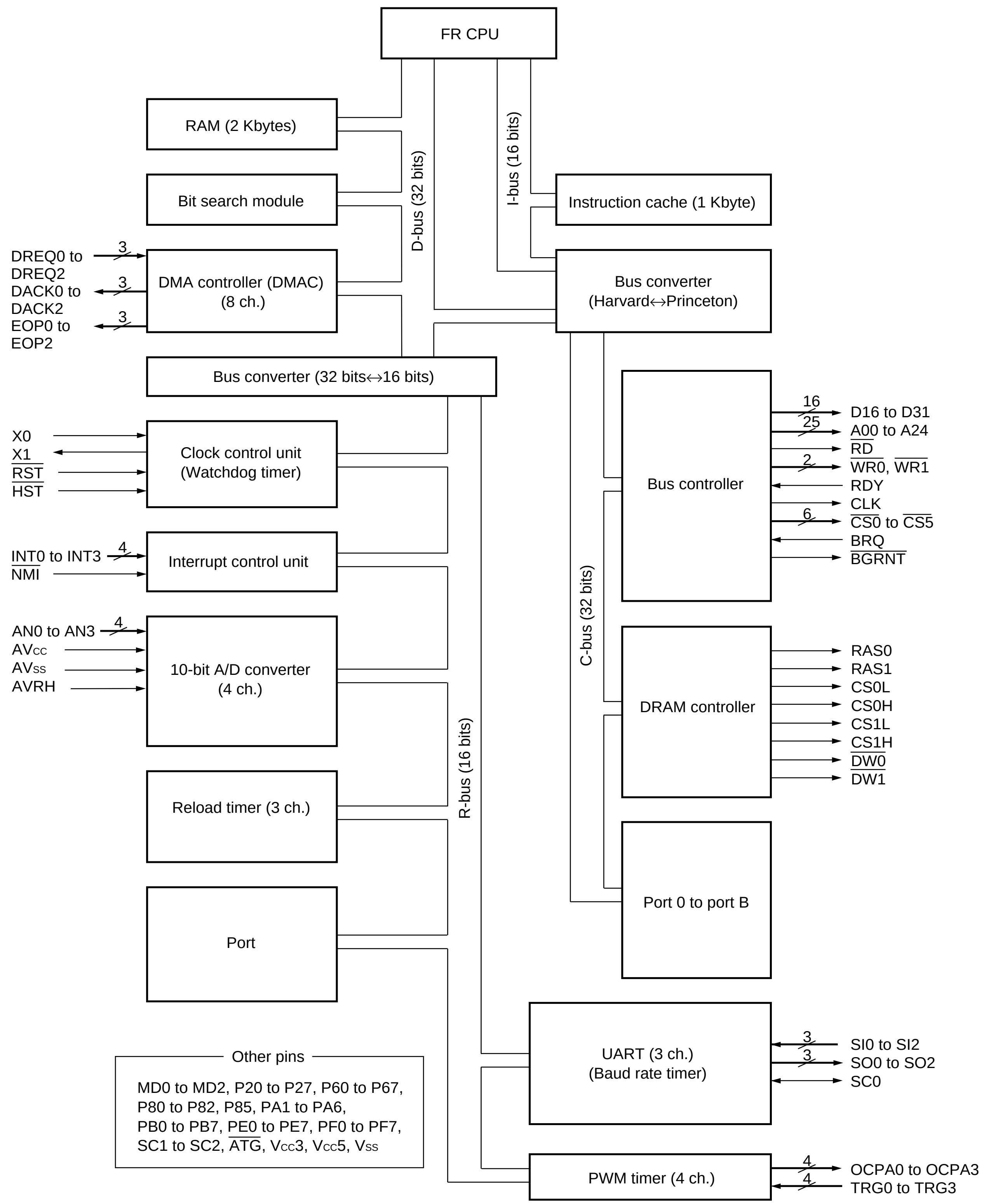
15. Hardware Stand-by at Turning on the Power Supply

When turning on the power supply with the $\overline{\text{HST}}$ pin being set to “L” level, the hardware doesn’t stand by. However the $\overline{\text{HST}}$ pin becomes available after the reset cancellation, the $\overline{\text{HST}}$ pin must once be back to “H” level.

16. Power on Reset

Make sure to make power on reset at turning on the power supply or returning on the power supply when the power supply voltage is below the warranty range for normal operation.

■ BLOCK DIAGRAM



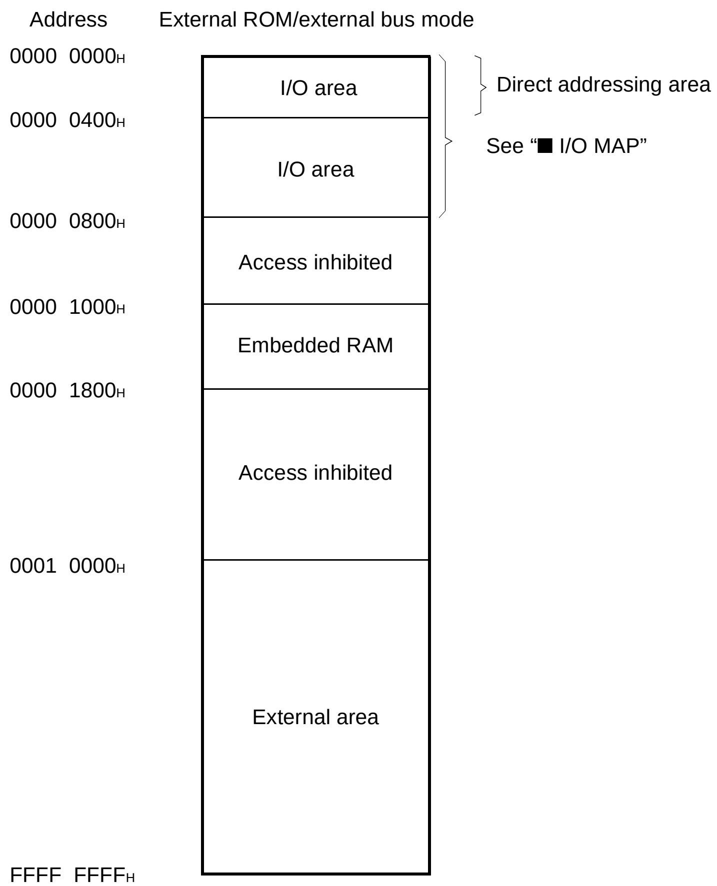
Note: Pins are display for functions (Actually some pins are multiplexer).
When using REALOS, time control should be done by using external interrupt or inner timer.

■ CPU CORE

1. Memory Space

The FR family has a logical address space of 4 Gbytes (2^{32} bytes) and the CPU linearly accesses the memory space.

- **Memory space**



- **Direct addressing area**

The following areas on the memory space are assigned to direct addressing area for I/O. In these areas, an address can be specified in a direct operand of a code.

Direct areas consists of the following areas dependent on accessible data sizes.

Byte data access: 000_H to $0FF_H$
Half word data access: 000_H to $1FF_H$
Word data access: 000_H to $3FF_H$

MB91101 Series

2. Registers

The FR family has two types of registers; dedicated registers embedded on the CPU and general-purpose registers on memory.

- **Dedicated registers**

Program counter (PC): 32-bit length, indicates the location of the instruction to be executed.
Program status (PS): 32-bit length, register for storing register pointer or condition codes
Table base register (TBR): Holds top address of vector table used in EIT (Exceptional/Interrupt/Trap) processing.
Return pointer (RP): Holds address to resume operation after returning from a subroutine.
System stack pointer (SSP): Indicates system stack space.
User's stack pointer (USP): Indicates user’s stack space.
Multiplication/division result register (MDH/MDL): 32-bit length, register for multiplication/division

32 bits		Initial value	
PC	Program counter	XXXX XXXXH	Indeterminate
PS	Program status		
TBR	Table base register	000F FC00H	
RP	Return pointer	XXXX XXXXH	Indeterminate
SSP	System stack pointer	0000 0000H	
USP	User’s stack pointer	XXXX XXXXH	Indeterminate
MDH	Multiplication/division result register	XXXX XXXXH	Indeterminate
MDL		XXXX XXXXH	Indeterminate

- **Program status (PS)**

The PS register is for holding program status and consists of a condition code register (CCR), a system condition code register (SCR) and a interrupt level mask register (ILM).

	31	20	19	18	17	16		10	9	8	7	6	5	4	3	2	1	0
PS	—	ILM4	ILM3	ILM2	ILM1	ILM0	—	D1	D0	T	—	—	S	I	N	Z	V	C
		ILM						SCR			CCR							

- **Condition code register (CCR)**

S-flag: Specifies a stack pointer used as R15.
I-flag: Controls user interrupt request enable/disable.
N-flag: Indicates sign bit when division result is assumed to be in the 2’s complement format.
Z-flag: Indicates whether or not the result of division was “0”.
V-flag: Assumes the operand used in calculation in the 2’s complement format and indicates whether or not overflow has occurred.
C-flag: Indicates if a carry or borrow from the MSB has occurred.

- **System condition code register (SCR)**

T-flag: Specifies whether or not to enable step trace trap.

- **Interrupt level mask register (ILM)**

ILM4 to ILM0: Register for holding interrupt level mask value. The value held by this register is used as a level mask. When an interrupt request issued to the CPU is higher than the level held by ILM, the interrupt request is accepted.

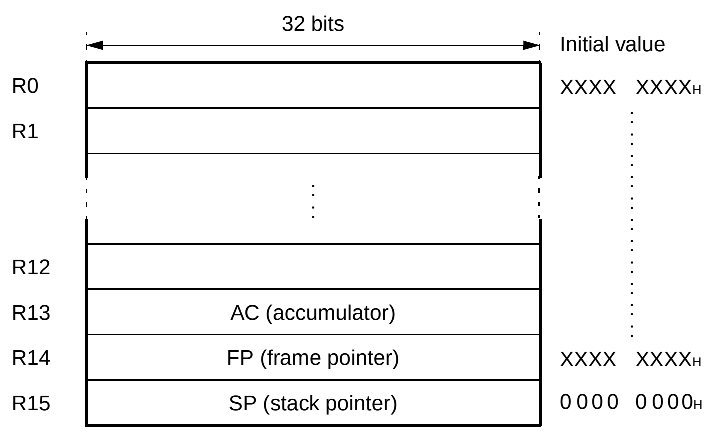
ILM4	ILM3	ILM2	ILM1	ILM0	Interrupt level	High-low
0	0	0	0	0	0	High
		⋮			⋮	↑
0	1	0	0	0	15	
		⋮			⋮	↓
1	1	1	1	1	31	Low

MB91101 Series

■ GENERAL-PURPOSE REGISTERS

R0 to R15 are general-purpose registers embedded on the CPU. These registers functions as an accumulator and a memory access pointer (field for indicating address).

• **Register bank structure**



Of the above 16 registers, following registers have special functions. To support the special functions, part of the instruction set has been sophisticated to have enhanced functions.

R13: Virtual accumulator (AC)
R14: Frame pointer (FP)
R15: Stack pointer (SP)

Upon reset, values in R0 to R14 are not fixed. Value in R15 is initialized to be 0000 0000_H (SSP value).

■ SETTING MODE

1. Pin

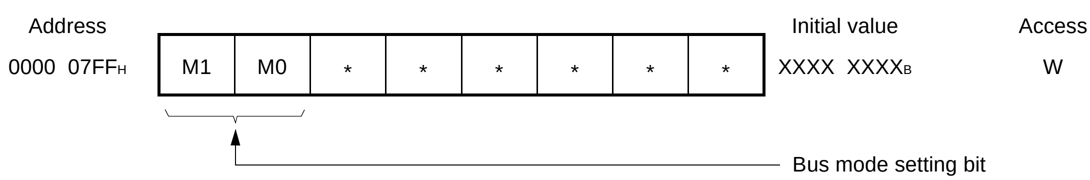
- **Mode setting pins and modes**

Mode setting pins			Mode name	Reset vector access area	External data bus width	Bus mode
MD2	MD1	MD0				
0	0	0	External vector mode 0	External	8 bits	External ROM/external bus mode
0	0	1	External vector mode 1	External	16 bits	
0	1	0	—	—	—	Inhibited
0	1	1	Internal vector mode	Internal	(Mode register)	Single-chip mode*
1	—	—	—	—	—	Inhibited

* : MB91101 does not support single-chip mode.

2. Registers

- **Mode setting registers (MODR) and modes**



W : Write only
X : Indeterminate
* : Always write “0” except for M1 and M0.

- **Bus mode setting bits and functions**

M1	M0	Functions	Note
0	0	Single-chip mode	
0	1	Internal ROM/external bus mode	
1	0	External ROM/external bus mode	
1	1	—	Inhibited

Note: Because of without internal ROM, MB91101 allows “10_B” setting value only.

MB91101 Series

■ I/O MAP

Address	Register name (abbreviated)	Register name	Read/write	Initial value
0000_H	(Vacancy)			
0001_H	PDR2	Port 2 data register	R/W	$XXXXXXXX_B$
0002_H to 0004_H	(Vacancy)			
0005_H	PDR6	Port 6 data register	R/W	$XXXXXXXX_B$
0006_H	(Vacancy)			
0007_H				
0008_H	PDRB	Port B data register	R/W	$XXXXXXXX_B$
0009_H	PDRA	Port A data register	R/W	$-XXXXXX-_B$
$000A_H$	(Vacancy)			
$000B_H$	PDR8	Port 8 data register	R/W	$--X--XXX_B$
$000C_H$ to 0011_H	(Vacancy)			
0012_H	PDRE	Port E data register	R/W	$XXXXXXXX_B$
0013_H	PDRF	Port F data register	R/W	$XXXXXXXX_B$
0014_H to $001B_H$	(Vacancy)			
$001C_H$	SSR0	Serial status register 0	R/W	$00001-00_B$
$001D_H$	SIDR0/SODR0	Serial input register 0/serial output register 0	R/W	$XXXXXXXX_B$
$001E_H$	SCR0	Serial control register 0	R/W	00000100_B
$001F_H$	SMR0	Serial mode register 0	R/W	$00--0-00_B$
0020_H	SSR1	Serial status register 1	R/W	$00001-00_B$
0021_H	SIDR1/SODR1	Serial input register 1/serial output register 1	R/W	$XXXXXXXX_B$
0022_H	SCR1	Serial control register 1	R/W	00000100_B
0023_H	SMR1	Serial mode register 1	R/W	$00--0-00_B$
0024_H	SSR2	Serial status register 2	R/W	$00001-00_B$
0025_H	SIDR2/SODR2	Serial input register 2/serial output register 2	R/W	$XXXXXXXX_B$
0026_H	SCR2	Serial control register 2	R/W	00000100_B
0027_H	SMR2	Serial mode register 2	R/W	$00--0-00_B$

(Continued)

Address	Register name (abbreviated)	Register name	Read/write	Initial value
0028H	TMRLR0	16-bit reload register ch. 0	W	XXXXXXXXB
0029H				XXXXXXXXB
002AH	TMR0	16-bit timer register ch. 0	R	XXXXXXXXB
002BH				XXXXXXXXB
002CH	(Vacancy)			
002DH				
002EH	TMCSR0	16-bit reload timer control status register ch. 0	R/W	––––0000B
002FH				00000000B
0030H	TMRLR1	16-bit reload register ch. 1	W	XXXXXXXXB
0031H				XXXXXXXXB
0032H	TMR1	16-bit timer register ch. 1	R	XXXXXXXXB
0033H				XXXXXXXXB
0034H	(Vacancy)			
0035H				
0036H	TMCSR1	16-bit reload timer control status register ch. 1	R/W	––––0000B
0037H				00000000B
0038H	ADCR	A/D converter data register	R	––––––XXB
0039H				XXXXXXXXB
003AH	ADCS	A/D converter control status register	R/W	00000000B
003BH				00000000B
003CH	TMRLR2	16-bit reload register ch. 2	W	XXXXXXXXB
003DH				XXXXXXXXB
003EH	TMR2	16-bit timer register ch. 2	R	XXXXXXXXB
003FH				XXXXXXXXB
0040H	(Vacancy)			
0041H				
0042H	TMCSR2	16-bit reload timer control status register ch. 2	R/W	––––0000B
0043H				00000000B
0044H to 0077H	(Vacancy)			

(Continued)

MB91101 Series

Address	Register name (abbreviated)	Register name	Read/write	Initial value
0078H	UTIM0/UTIMR0	U-TIMER register ch. 0/reload register ch. 0	R/W	0 0 0 0 0 0 0 0 B
0079H				0 0 0 0 0 0 0 0 B
007AH	(Vacancy)			
007BH	UTIMC0	U-TIMER control register ch. 0	R/W	0 – – 0 0 0 0 1 B
007CH	UTIM1/UTIMR1	U-TIMER register ch. 1/reload register ch. 1	R/W	0 0 0 0 0 0 0 0 B
007DH				0 0 0 0 0 0 0 0 B
007EH	(Vacancy)			
007FH	UTIMC1	U-TIMER control register ch. 1	R/W	0 – – 0 0 0 0 1 B
0080H	UTIM2/UTIMR2	U-TIMER register ch. 2/reload register ch. 0	R/W	0 0 0 0 0 0 0 0 B
0081H				0 0 0 0 0 0 0 0 B
0082H	(Vacancy)			
0083H	UTIMC2	U-TIMER control register ch. 2	R/W	0 – – 0 0 0 0 1 B
0084H to 0093H	(Vacancy)			
0094H	EIRR	External interrupt cause register	R/W	0 0 0 0 0 0 0 0 B
0095H	ENIR	Interrupt enable register	R/W	0 0 0 0 0 0 0 0 B
0096H to 0098H	(Vacancy)			
0099H	ELVR	External interrupt request level setting register	R/W	0 0 0 0 0 0 0 0 B
009AH to 00D1H	(Vacancy)			
00D2H	DDRE	Port E data direction register	W	0 0 0 0 0 0 0 0 B
00D3H	DDRF	Port F data direction register	W	0 0 0 0 0 0 0 0 B
00D4H to 00DBH	(Vacancy)			
00DCH	GCN1	General control register 1	R/W	0 0 1 1 0 0 1 0 B
00DDH				0 0 0 1 0 0 0 0 B
00DEH	(Vacancy)			
00DFH	GCN2	General control register 2	R/W	0 0 0 0 0 0 0 0 B

(Continued)

Address	Register name (abbreviated)	Register name	Read/write	Initial value
00E0H	PTMR0	Ch. 0 timer register	R	11111111B
00E1H				11111111B
00E2H	PCSR0	Ch. 0 cycle setting register	W	XXXXXXXXB
00E3H				XXXXXXXXB
00E4H	PDUT0	Ch. 0 duty setting register	W	XXXXXXXXB
00E5H				XXXXXXXXB
00E6H	PCNH0	Ch. 0 control status register H	R/W	0000000–B
00E7H	PCNL0	Ch. 0 control status register L	R/W	00000000B
00E8H	PTMR1	Ch. 1 timer register	R	11111111B
00E9H				11111111B
00EAH	PCSR1	Ch. 1 cycle setting register	W	XXXXXXXXB
00EBH				XXXXXXXXB
00ECH	PDUT1	Ch. 1 duty setting register	W	XXXXXXXXB
00EDH				XXXXXXXXB
00EEH	PCNH1	Ch. 1 control status register H	R/W	0000000–B
00EFH	PCNL1	Ch. 1 control status register L	R/W	00000000B
00F0H	PTMR2	Ch. 2 timer register	R	11111111B
00F1H				11111111B
00F2H	PCSR2	Ch. 2 cycle setting register	W	XXXXXXXXB
00F3H				XXXXXXXXB
00F4H	PDUT2	Ch. 2 duty setting register	W	XXXXXXXXB
00F5H				XXXXXXXXB
00F6H	PCNH2	Ch. 2 control status register H	R/W	0000000–B
00F7H	PCNL2	Ch. 2 control status register L	R/W	00000000B
00F8H	PTMR3	Ch. 3 timer register	R	11111111B
00F9H				11111111B
00FAH	PCSR3	Ch. 3 cycle setting register	W	XXXXXXXXB
00FBH				XXXXXXXXB
00FCH	PDUT3	Ch. 3 duty setting register	W	XXXXXXXXB
00FDH				XXXXXXXXB
00FEH	PCNH3	Ch. 3 control status register H	R/W	0000000–B
00FFH	PCNL3	Ch. 3 control status register L	R/W	00000000B

(Continued)

MB91101 Series

Address	Register name (abbreviated)	Register name	Read/write	Initial value
0100H to 01FFH	(Vacancy)			
0200H	DPDP	DMAC parameter descriptor pointer	R/W	XXXXXXXXB
0201H				XXXXXXXXB
0202H				XXXXXXXXB
0203H				X0000000B
0204H	DACSR	DMAC control status register	R/W	00000000B
0205H				00000000B
0206H				00000000B
0207H				00000000B
0208H	DATCR	DMAC pin control register	R/W	XXXXXXXXB
0209H				XXXX0000B
020AH				XXXX0000B
020BH				XXXX0000B
020CH to 03E3H	(Vacancy)			
03E4H	ICHCR	Instruction cache control register	R/W	––––––––B
03E5H				––––––––B
03E6H				––––––––B
03E7H				––000000B
03E8H to 03EFH	(Vacancy)			
03F0H	BSD0	Bit search module 0-detection data register	W	XXXXXXXXB
03F1H				XXXXXXXXB
03F2H				XXXXXXXXB
03F3H				XXXXXXXXB
03F4H	BSD1	Bit search module 1-detection data register	R/W	XXXXXXXXB
03F5H				XXXXXXXXB
03F6H				XXXXXXXXB
03F7H				XXXXXXXXB

(Continued)

Address	Register name (abbreviated)	Register name	Read/write	Initial value
03F8H	BSDC	Bit search module transition-detection data register	W	XXXXXXXXB
03F9H				XXXXXXXXB
03FAH				XXXXXXXXB
03FBH				XXXXXXXXB
03FCH	BSRR	Bit search module detection result register	R	XXXXXXXXB
03FDH				XXXXXXXXB
03FEH				XXXXXXXXB
03FFH				XXXXXXXXB
0400H	ICR00	Interrupt control register 0	R/W	– – – 1 1 1 1 1B
0401H	ICR01	Interrupt control register 1	R/W	– – – 1 1 1 1 1B
0402H	ICR02	Interrupt control register 2	R/W	– – – 1 1 1 1 1B
0403H	ICR03	Interrupt control register 3	R/W	– – – 1 1 1 1 1B
0404H	ICR04	Interrupt control register 4	R/W	– – – 1 1 1 1 1B
0405H	ICR05	Interrupt control register 5	R/W	– – – 1 1 1 1 1B
0406H	ICR06	Interrupt control register 6	R/W	– – – 1 1 1 1 1B
0407H	ICR07	Interrupt control register 7	R/W	– – – 1 1 1 1 1B
0408H	ICR08	Interrupt control register 8	R/W	– – – 1 1 1 1 1B
0409H	ICR09	Interrupt control register 9	R/W	– – – 1 1 1 1 1B
040AH	ICR10	Interrupt control register 10	R/W	– – – 1 1 1 1 1B
040BH	ICR11	Interrupt control register 11	R/W	– – – 1 1 1 1 1B
040CH	ICR12	Interrupt control register 12	R/W	– – – 1 1 1 1 1B
040DH	ICR13	Interrupt control register 13	R/W	– – – 1 1 1 1 1B
040EH	ICR14	Interrupt control register 14	R/W	– – – 1 1 1 1 1B
040FH	ICR15	Interrupt control register 15	R/W	– – – 1 1 1 1 1B
0410H	ICR16	Interrupt control register 16	R/W	– – – 1 1 1 1 1B
0411H	ICR17	Interrupt control register 17	R/W	– – – 1 1 1 1 1B
0412H	ICR18	Interrupt control register 18	R/W	– – – 1 1 1 1 1B
0413H	ICR19	Interrupt control register 19	R/W	– – – 1 1 1 1 1B
0414H	ICR20	Interrupt control register 20	R/W	– – – 1 1 1 1 1B
0415H	ICR21	Interrupt control register 21	R/W	– – – 1 1 1 1 1B
0416H	ICR22	Interrupt control register 22	R/W	– – – 1 1 1 1 1B

(Continued)

MB91101 Series

Address	Register name (abbreviated)	Register name	Read/write	Initial value
0417H	ICR23	Interrupt control register 23	R/W	– – – 1 1 1 1 1 B
0418H	ICR24	Interrupt control register 24	R/W	– – – 1 1 1 1 1 B
0419H	ICR25	Interrupt control register 25	R/W	– – – 1 1 1 1 1 B
041AH	ICR26	Interrupt control register 26	R/W	– – – 1 1 1 1 1 B
041BH	ICR27	Interrupt control register 27	R/W	– – – 1 1 1 1 1 B
041CH	ICR28	Interrupt control register 28	R/W	– – – 1 1 1 1 1 B
041DH	ICR29	Interrupt control register 29	R/W	– – – 1 1 1 1 1 B
041EH	ICR30	Interrupt control register 30	R/W	– – – 1 1 1 1 1 B
041FH	ICR31	Interrupt control register 31	R/W	– – – 1 1 1 1 1 B
042FH	ICR47	Interrupt control register 47	R/W	– – – 1 1 1 1 1 B
0430H	DICR	Delayed interrupt control register	R/W	– – – – – – – 0 B
0431H	HRCL	Hold request cancel request level setting register	R/W	– – – 1 1 1 1 1 B
0432H to 047FH	(Vacancy)			
0480H	RSRR/WTCR	Reset cause register/ watchdog peripheral control register	R/W	1X X X X – 0 0 B
0481H	STCR	Standby control register	R/W	0 0 0 1 1 1 – – B
0482H	PDRR	DMA controller request squelch register	R/W	– – – – 0 0 0 0 B
0483H	CTBR	Timebase timer clear register	W	X X X X X X X X B
0484H	GCR	Gear control register	R/W	1 1 0 0 1 1 – 1 B
0485H	WPR	Watchdog reset occurrence postpone register	W	X X X X X X X X B
0486H	(Vacancy)			
0487H				
0488H	PCTR	PLL control register	R/W	0 0 – – 0 – – – B
0489H to 0600H	(Vacancy)			
0601H	DDR2	Port 2 data direction register	W	0 0 0 0 0 0 0 0 B
0602H to 0604H	(Vacancy)			
0605H	DDR6	Port 6 data direction register	W	0 0 0 0 0 0 0 0 B
0606H	(Vacancy)			
0607H				

(Continued)

Address	Register name (abbreviated)	Register name	Read/write	Initial value
0608H	DDRB	Port B data direction register	W	0 0 0 0 0 0 0 0B
0609H	DDRA	Port A data direction register	W	– 0 0 0 0 0 0 –B
060AH	(Vacancy)			
060BH	DDR8	Port 8 data direction register	W	– – 0 – – 0 0 0B
060CH	ASR1	Area select register 1	W	0 0 0 0 0 0 0 0B
060DH				0 0 0 0 0 0 0 1B
060EH	AMR1	Area mask register 1	W	0 0 0 0 0 0 0 0B
060FH				0 0 0 0 0 0 0 0B
0610H	ASR2	Area select register 2	W	0 0 0 0 0 0 0 0B
0611H				0 0 0 0 0 0 1 0B
0612H	AMR2	Area mask register 2	W	0 0 0 0 0 0 0 0B
0613H				0 0 0 0 0 0 0 0B
0614H	ASR3	Area select register 3	W	0 0 0 0 0 0 0 0B
0615H				0 0 0 0 0 0 1 1B
0616H	AMR3	Area mask register 3	W	0 0 0 0 0 0 0 0B
0617H				0 0 0 0 0 0 0 0B
0618H	ASR4	Area select register 4	W	0 0 0 0 0 0 0 0B
0619H				0 0 0 0 0 1 0 0B
061AH	AMR4	Area mask register 4	W	0 0 0 0 0 0 0 0B
061BH				0 0 0 0 0 0 0 0B
061CH	ASR5	Area select register 5	W	0 0 0 0 0 0 0 0B
061DH				0 0 0 0 0 1 0 1B
061EH	AMR5	Area mask register 5	W	0 0 0 0 0 0 0 0B
061FH				0 0 0 0 0 0 0 0B
0620H	AMD0	Area mode register 0	R/W	– – – 0 0 1 1 1B
0621H	AMD1	Area mode register 1	R/W	0 – – 0 0 0 0 0B
0622H	AMD32	Area mode register 32	R/W	0 0 0 0 0 0 0 0B
0623H	AMD4	Area mode register 4	R/W	0 – – 0 0 0 0 0B
0624H	AMD5	Area mode register 5	R/W	0 – – 0 0 0 0 0B
0625H	DSCR	DRAM signal control register	W	0 0 0 0 0 0 0 0B
0626H	RFCR	Refresh control register	R/W	– – X X X X X XB
0627H				0 0 – – – 0 0 0B

(Continued)

MB91101 Series

(Continued)

Address	Register name (abbreviated)	Register name	Read/write	Initial value
0628H	EPCR0	External pin control register 0	W	– – – – 1 1 0 0 B
0629H				– 1 1 1 1 1 1 1 B
062AH	(Vacancy)			
062BH	EPCR1	External pin control register 1	W	1 1 1 1 1 1 1 1 B
062CH	DMCR4	DRAM control register 4	R/W	0 0 0 0 0 0 0 0 B
062DH				0 0 0 0 0 0 0 – B
062EH	DMCR5	DRAM control register 5	R/W	0 0 0 0 0 0 0 0 B
062FH				0 0 0 0 0 0 0 – B
0630H to 07FDH	(Vacancy)			
07FEH	LER	Little endian register	W	– – – – – 0 0 0 B
07FFH	MODR	Mode register	W	X X X X X X X X B

Note: Do not use (vacancy).

■ INTERRUPT CAUSES, INTERRUPT VECTORS AND INTERRUPT CONTROL REGISTER ALLOCATIONS

Interrupt causes	Interrupt number		Interrupt level		TBR default address
	Decimal	Hexadecimal	Register	Offset	
Reset	0	00	—	3FCH	000FFFFCH
Reserved for system	1	01	—	3F8H	000FFFF8H
Reserved for system	2	02	—	3F4H	000FFFF4H
Reserved for system	3	03	—	3F0H	000FFFF0H
Reserved for system	4	04	—	3ECH	000FFFECH
Reserved for system	5	05	—	3E8H	000FFFE8H
Reserved for system	6	06	—	3E4H	000FFFE4H
Reserved for system	7	07	—	3E0H	000FFFE0H
Reserved for system	8	08	—	3DCH	000FFFDCH
Reserved for system	9	09	—	3D8H	000FFFD8H
Reserved for system	10	0A	—	3D4H	000FFFD4H
Reserved for system	11	0B	—	3D0H	000FFFD0H
Reserved for system	12	0C	—	3CCH	000FFFCCH
Reserved for system	13	0D	—	3C8H	000FFFC8H
Exception for undefined instruction	14	0E	—	3C4H	000FFFC4H
NMI request	15	0F	FH fixed	3C0H	000FFFC0H
External interrupt 0	16	10	ICR00	3BCH	000FFFBCH
External interrupt 1	17	11	ICR01	3B8H	000FFFB8H
External interrupt 2	18	12	ICR02	3B4H	000FFFB4H
External interrupt 3	19	13	ICR03	3B0H	000FFFB0H
UART0 receive complete	20	14	ICR04	3ACH	000FFFACH
UART1 receive complete	21	15	ICR05	3A8H	000FFFA8H
UART2 receive complete	22	16	ICR06	3A4H	000FFFA4H
UART0 transmit complete	23	17	ICR07	3A0H	000FFFA0H
UART1 transmit complete	24	18	ICR08	39CH	000FFF9CH
UART2 transmit complete	25	19	ICR09	398H	000FFF98H
DMAC0 (complete, error)	26	1A	ICR10	394H	000FFF94H
DMAC1 (complete, error)	27	1B	ICR11	390H	000FFF90H
DMAC2 (complete, error)	28	1C	ICR12	38CH	000FFF8CH
DMAC3 (complete, error)	29	1D	ICR13	388H	000FFF88H
DMAC4 (complete, error)	30	1E	ICR14	384H	000FFF84H
DMAC5 (complete, error)	31	1F	ICR15	380H	000FFF80H

(Continued)

MB91101 Series

Interrupt causes	Interrupt number		Interrupt level		TBR default address
	Decimal	Hexadecimal	Register	Offset	
DMAC6 (complete, error)	32	20	ICR16	37CH	000FFF7CH
DMAC7 (complete, error)	33	21	ICR17	378H	000FFF78H
A/D converter (successive approximation conversion type)	34	22	ICR18	374H	000FFF74H
16-bit reload timer 0	35	23	ICR19	370H	000FFF70H
16-bit reload timer 1	36	24	ICR20	36CH	000FFF6CH
16-bit reload timer 2	37	25	ICR21	368H	000FFF68H
PWM 0	38	26	ICR22	364H	000FFF64H
PWM 1	39	27	ICR23	360H	000FFF60H
PWM 2	40	28	ICR24	35CH	000FFF5CH
PWM 3	41	29	ICR25	358H	000FFF58H
U-TIMER 0	42	2A	ICR26	354H	000FFF54H
U-TIMER 1	43	2B	ICR27	350H	000FFF50H
U-TIMER 2	44	2C	ICR28	34CH	000FFF4CH
Reserved for system	45	2D	ICR29	348H	000FFF48H
Reserved for system	46	2E	ICR30	344H	000FFF44H
Reserved for system	47	2F	ICR31	340H	000FFF40H
Reserved for system	48	30	ICR32	33CH	000FFF3CH
Reserved for system	49	31	ICR33	338H	000FFF38H
Reserved for system	50	32	ICR34	334H	000FFF34H
Reserved for system	51	33	ICR35	330H	000FFF30H
Reserved for system	52	34	ICR36	32CH	000FFF2CH
Reserved for system	53	35	ICR37	328H	000FFF28H
Reserved for system	54	36	ICR38	324H	000FFF24H
Reserved for system	55	37	ICR39	320H	000FFF20H
Reserved for system	56	38	ICR40	31CH	000FFF1CH
Reserved for system	57	39	ICR41	318H	000FFF18H
Reserved for system	58	3A	ICR42	314H	000FFF14H
Reserved for system	59	3B	ICR43	310H	000FFF10H
Reserved for system	60	3C	ICR44	30CH	000FFF0CH
Reserved for system	61	3D	ICR45	308H	000FFF08H
Reserved for system	62	3E	ICR46	304H	000FFF04H
Delayed interrupt cause bit	63	3F	ICR47	300H	000FFF00H

(Continued)

(Continued)

Interrupt causes	Interrupt number		Interrupt level		TBR default address
	Decimal	Hexadecimal	Register	Offset	
Reserved for system (used in REALOS*)	64	40	—	2FCH	000FFEFCH
Reserved for system (used in REALOS*)	65	41	—	2F8H	000FFEF8H
Used in INT instructions	66 to 255	42 to FF	—	2F4H to 000H	000FFEF4H to 000FFC00H

* : When using in REALOS/FR, interrupt 0x40, 0x41 for system code.

MB91101 Series

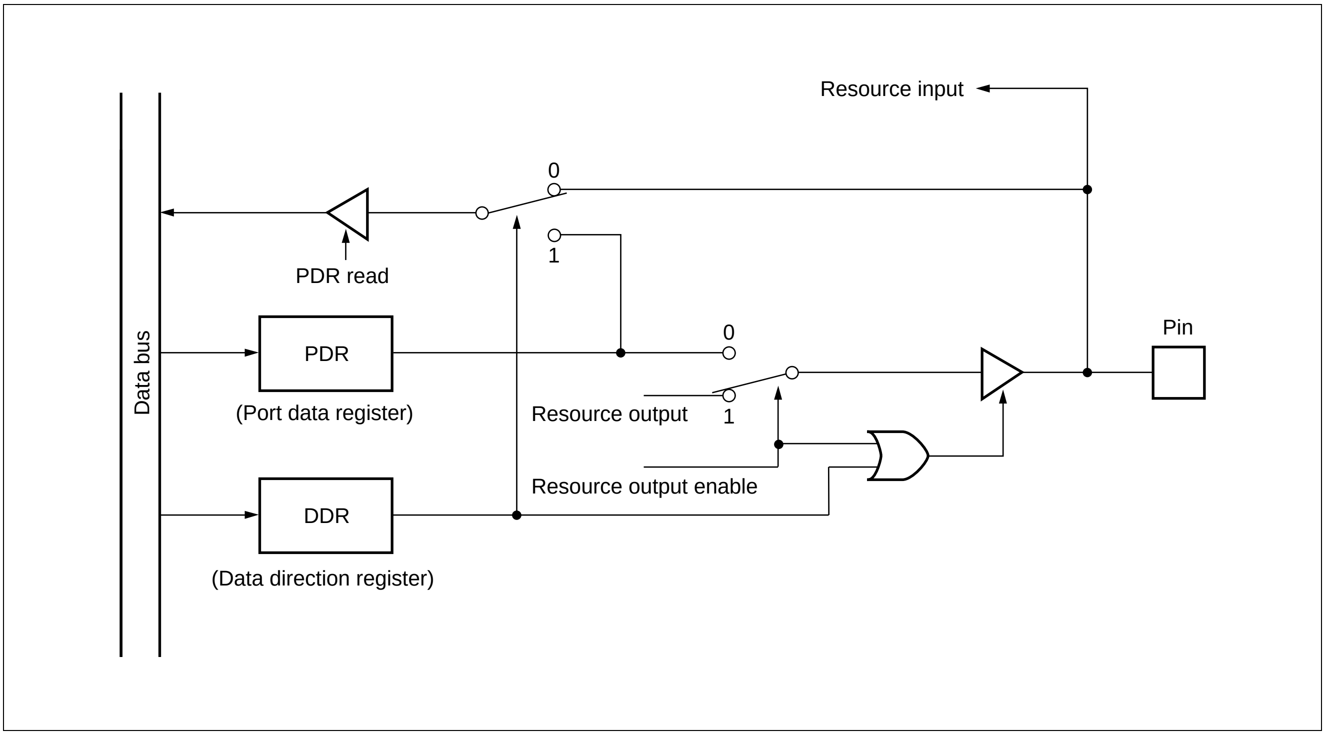
■ PERIPHERAL RESOURCES

1. I/O Ports

There are 2 types of I/O port register structure; port data register (PDR0 to PDRF) and data direction register (DDR0 to DDRF), where bits PDR0 to PDRF and bits DDR0 to DDRF corresponds respectively. Each bit on the register corresponds to an external pin. In port registers input/output register of the port configures input/output function of the port, while corresponding bit (pin) configures input/output function in data direction registers. Bit “0” specifies input and “1” specifies output.

- For input (DDR = “0”) setting;
  PDR reading operation: reads level of corresponding external pin.
  PDR writing operation: writes set value to PDR.
- For output (DDR = “1”) setting;
  PDR reading operation: reads PDR value.
  PDR writing operation: outputs PDR value to corresponding external pin.

- **Block diagram**



- **Port data register**

Address	bit 7 — bit 0	Initial value	
000001H	PDR1	XXXXXXXX B	(R/W)
000005H	PDR6	XXXXXXXX B	(R/W)
00000BH	PDR8	- - X - - XXX B	(R/W)
000009H	PDRA	- XXXXXX - B	(R/W)
000008H	PDRB	XXXXXXXX B	(R/W)
000012H	PDRE	XXXXXXXX B	(R/W)
000013H	PDRF	XXXXXXXX B	(R/W)

( ) : Access
R/W : Readable and writable
X : Indeterminate

- **Data direction register**

Address	bit 7 — bit 0	Initial value	
000601H	DDR2	00000000 B	(W)
000605H	DDR6	00000000 B	(W)
00060BH	DDR8	- - 0 - - 000 B	(W)
000609H	DDRA	- 000000 - B	(W)
000608H	DDRB	00000000 B	(W)
0000D2H	DDRE	00000000 B	(W)
0000D3H	DDRF	00000000 B	(W)

( ) : Access
W : Write only
– : Unused

MB91101 Series

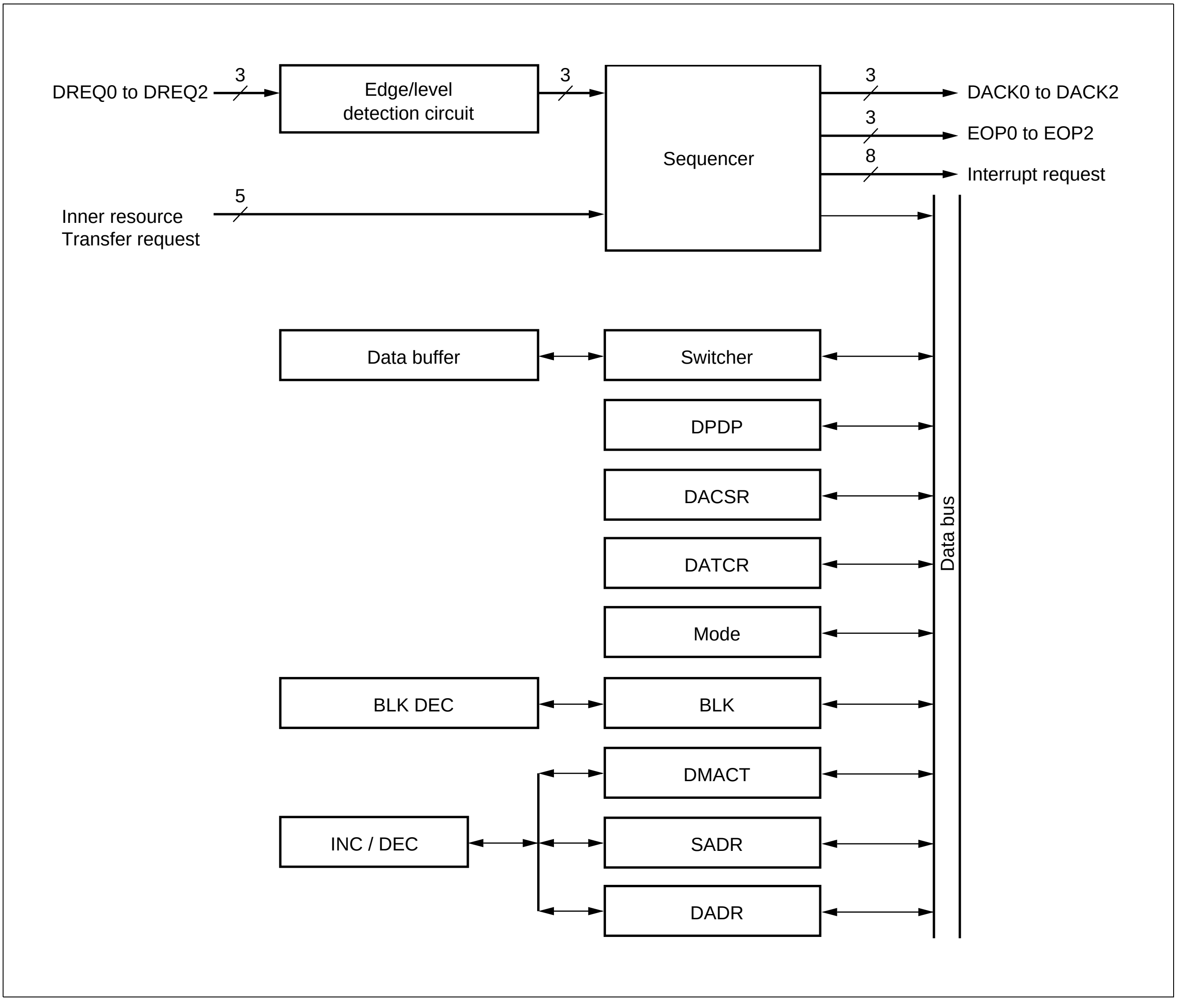
2. DMA Controller (DMAC)

The DMA controller is a module embedded in FR family devices, and performs DMA (direct memory access) transfer.

DMA transfer performed by the DMA controller transfers data without intervention of CPU, contributing to enhanced performance of the system.

- 8 channels
- Mode: single/block transfer, burst transfer and continuous transfer: 3 kinds of transfer
- Transfer all through the area
- Max. 65536 of transfer cycles
- Interrupt function right after the transfer
- Selectable for address transfer increase/decrease by the software
- External transfer request input pin, external transfer request accept output pin, external transfer complete output pin three pins for each

- **Block diagram**



• Registers (DMAC internal registers)

Address	bit 31 … bit 16 … bit 0	Initial value	
00000200H	DPDP	XXXXXXXXB	(R/W)
00000201H		XXXXXXXXB	
00000202H		XXXXXXXXB	
00000203H		X0000000B	
00000204H	DACSR	00000000B	(R/W)
00000205H		00000000B	
00000206H		00000000B	
00000207H		00000000B	
00000208H	DATCR	XXXXXXXXB	(R/W)
00000209H		XXXX0000B	
0000020AH		XXXX0000B	
0000020BH		XXXX0000B	

( ) : Access
R/W : Readable and writable
X : Indeterminate

• Registers (DMA descriptor)

Address	bit 31 … bit 0	
DPDP + 0H		DMA ch.0 Descriptor
DPDP + 0CH		DMA ch.1 Descriptor
⋮	⋮	
DPDP + 54H		DMA ch.7 Descriptor

MB91101 Series

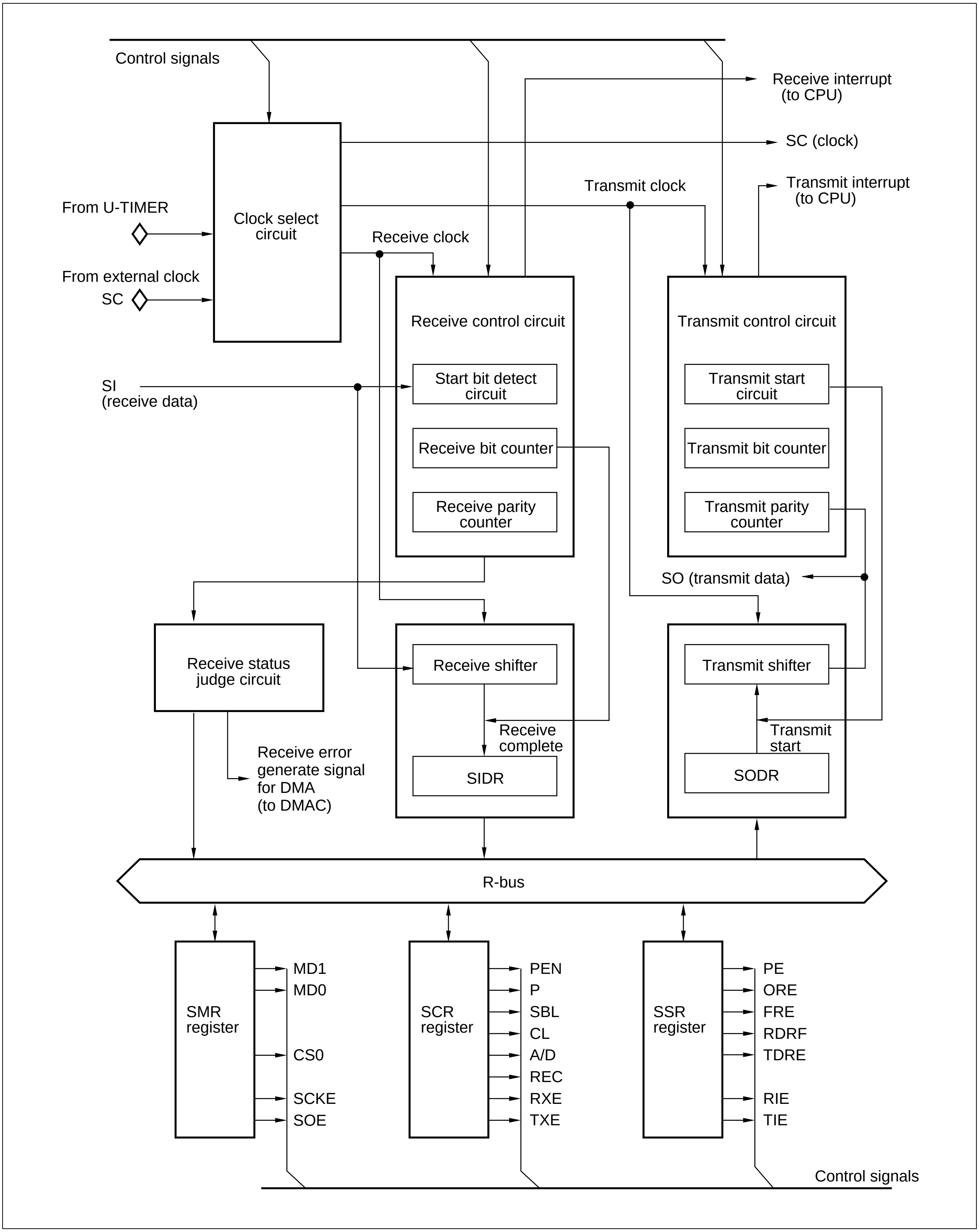
3. UART

The UART is a serial I/O port for supporting asynchronous (start-stop system) communication or CLK synchronous communication, and it has the following features.

The MB91101 consists of 3 channels of UART.

- Full double double buffer
- Both a synchronous (start-stop system) communication and CLK synchronous communication are available.
- Supporting multi-processor mode
- Perfect programmable baud rate
  Any baud rate can be set by internal timer (refer to section “4. U-TIMER”).
- Any baud rate can be set by external clock.
- Error checking function (parity, framing and overrun)
- Transfer signal: NRZ code
- Enable DMA transfer/start by interrupt.

• **Block diagram**



- **Register configuration**

Address	bit 15 – bit 8	bit 7 – bit 0	Initial value	
0000001EH	SCR0		0 0 0 0 0 1 0 0 B	(R/W)
00000022H	SCR1		0 0 0 0 0 1 0 0 B	(R/W)
00000026H	SCR2		0 0 0 0 0 1 0 0 B	(R/W)
0000001FH		SMR0	0 0 - - 0 - 0 0 B	(R/W)
00000023H		SMR1	0 0 - - 0 - 0 0 B	(R/W)
00000027H		SMR2	0 0 - - 0 - 0 0 B	(R/W)
0000001CH	SSR0		0 0 0 0 1 - 0 0 B	(R/W)
00000020H	SSR1		0 0 0 0 1 - 0 0 B	(R/W)
00000024H	SSR2		0 0 0 0 1 - 0 0 B	(R/W)
0000001DH		SIDR0/SODR0	X X X X X X X X B	(R/W)
00000021H		SIDR1/SIDR1	X X X X X X X X B	(R/W)
00000025H		SIDR2/SIDR2	X X X X X X X X B	(R/W)

( ) : Access
R/W : Readable and writable
– : Unused
X : Indeterminate

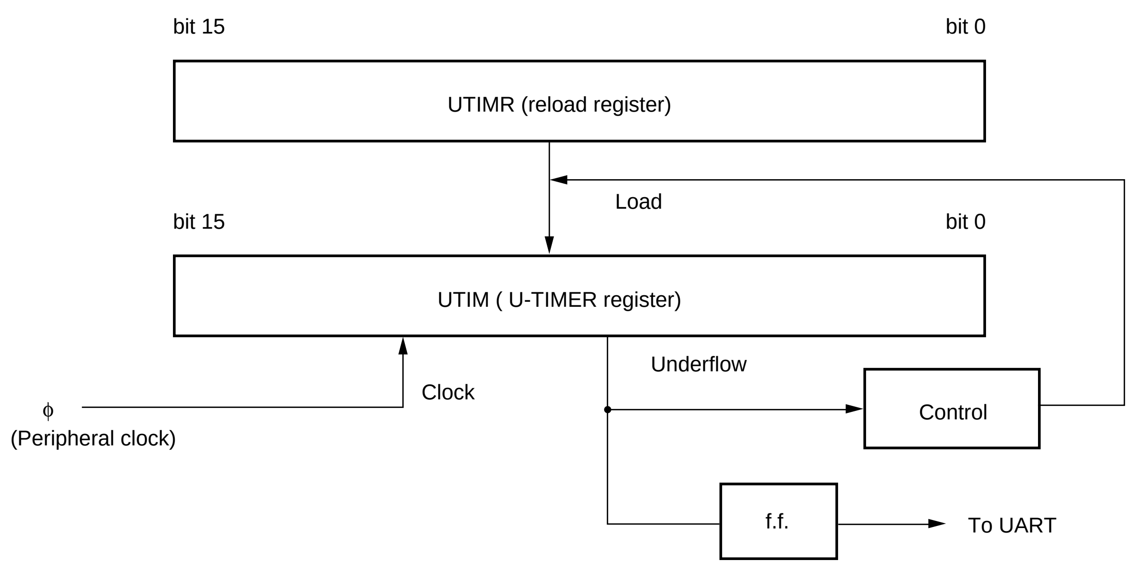
4. U-TIMER (16-bit Timer for UART Baud Rate Generation)

The U-TIMER is a 16-bit timer for generating UART baud rate. Combination of chip operating frequency and reload value of U-TIMER allows flexible setting of baud rate.

The U-TIMER operates as an interval timer by using interrupt issued on counter underflow.

The MB91101 has 3 channel U-TIMER embedded on the chip. An interval of up to $2^{16} \times \phi$ can be counted.

- **Block diagram**



- **Register configuration**

Address	bit 15 … bit 0	Initial value	
00000078H 00000079H	UTIM0/UTIMR0	0 0 0 0 0 0 0 0 B 0 0 0 0 0 0 0 0 B	(R/W)
0000007CH 0000007DH	UTIM1/UTIMR1	0 0 0 0 0 0 0 0 B 0 0 0 0 0 0 0 0 B	(R/W)
00000080H 00000081H	UTIM2/UTIMR2	0 0 0 0 0 0 0 0 B 0 0 0 0 0 0 0 0 B	(R/W)
0000007BH	UTIMC0	0 - - 0 0 0 0 1 B	(R/W)
0000007FH	UTIMC1	0 - - 0 0 0 0 1 B	(R/W)
00000083H	UTIMC2	0 - - 0 0 0 0 1 B	(R/W)

( ) : Access
R/W : Readable and writable
– : Unused

MB91101 Series

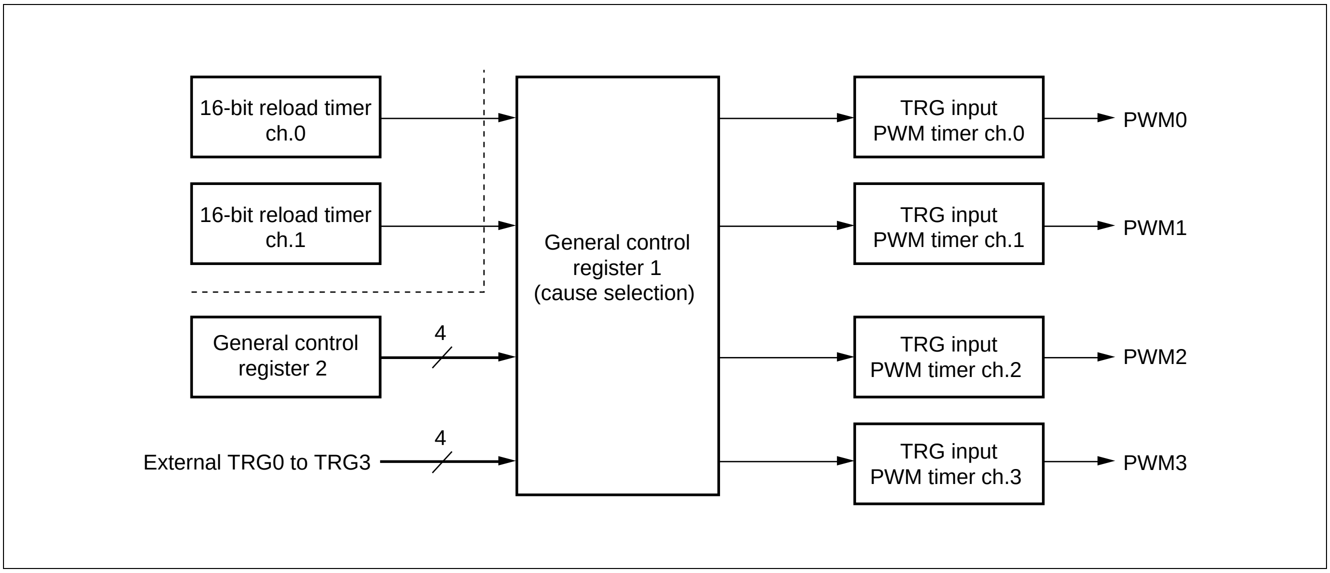
5. PWM Timer

The PWM timer can output high accurate PWM waves efficiently.

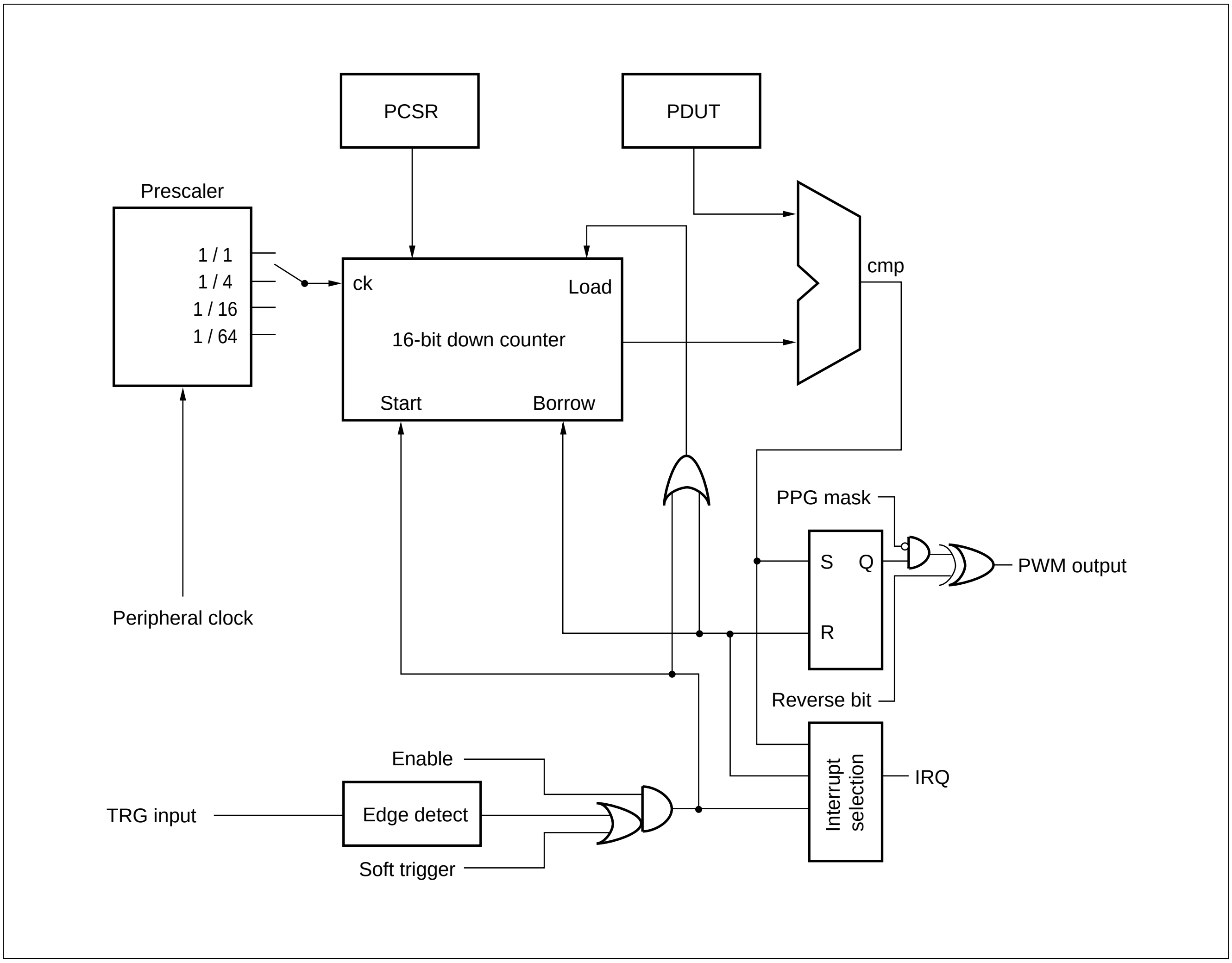
MB91101 has inner 4-channel PWM timers, and has the following features.

- Each channel consists of a 16-bit down counter, a 16-bit data resister with a buffer for scyde setting, a 16-bit compare resister with a buffer for duty setting, and a pin controller.
- The count clock of a 16-bit down counter can be selected from the following four inner clocks.
  Inner clock ϕ, $\phi/4$, $\phi/16$, $\phi/64$
- The counter value can be initialized "FFFFH" by the resetting or the counter borrow.
- PWM output (each channel)
- Resister description

- **Block diagram (general construction)**



• **Block diagram (for one channel)**



MB91101 Series

- **Register configuration**

Address	bit 15 … bit 8 … bit 0	Initial value	Access
000000DCH 000000DDH	GCN1	0 0 1 1 0 0 1 0 B 0 0 0 1 0 0 0 0 B	(R/W)
000000DFH	GCN2	0 0 0 0 0 0 0 0 B	(R/W)
000000E0H 000000E1H	PTMR0	1 1 1 1 1 1 1 1 B 1 1 1 1 1 1 1 1 B	(R)
000000E2H 000000E3H	PCSR0	X X X X X X X X B X X X X X X X X B	(W)
000000E4H 000000E5H	PDUT0	X X X X X X X X B X X X X X X X X B	(W)
000000E6H	PCNH0	0 0 0 0 0 0 0 - B	(R/W)
000000E7H	PCNL0	0 0 0 0 0 0 0 0 B	(R/W)
000000E8H 000000E9H	PTMR1	1 1 1 1 1 1 1 1 B 1 1 1 1 1 1 1 1 B	(R)
000000EAH 000000EBH	PCSR1	X X X X X X X X B X X X X X X X X B	(W)
000000ECH 000000EDH	PDUT1	X X X X X X X X B X X X X X X X X B	(W)
000000EEH	PCNH1	0 0 0 0 0 0 0 - B	(R/W)
000000EFH	PCNL1	0 0 0 0 0 0 0 0 B	(R/W)
000000F0H 000000F1H	PTMR2	1 1 1 1 1 1 1 1 B 1 1 1 1 1 1 1 1 B	(R)
000000F2H 000000F3H	PCSR2	X X X X X X X X B X X X X X X X X B	(W)
000000F4H 000000F5H	PDUT2	X X X X X X X X B X X X X X X X X B	(W)
000000F6H	PCNH2	0 0 0 0 0 0 0 - B	(R/W)
000000F7H	PCNL2	0 0 0 0 0 0 0 0 B	(R/W)
000000F8H 000000F9H	PTMR3	1 1 1 1 1 1 1 1 B 1 1 1 1 1 1 1 1 B	(R)
000000FAH 000000FBH	PCSR3	X X X X X X X X B X X X X X X X X B	(W)
000000FCH 000000FDH	PDUT3	X X X X X X X X B X X X X X X X X B	(W)
000000FEH	PCNH3	0 0 0 0 0 0 0 - B	(R/W)
000000FFH	PCNL3	0 0 0 0 0 0 0 0 B	(R/W)

( ) : Access
R/W : Readable and writable
R : Read only
W : Write only
– : Unused
X : Indeterminate

6. 16-bit Reload Timer

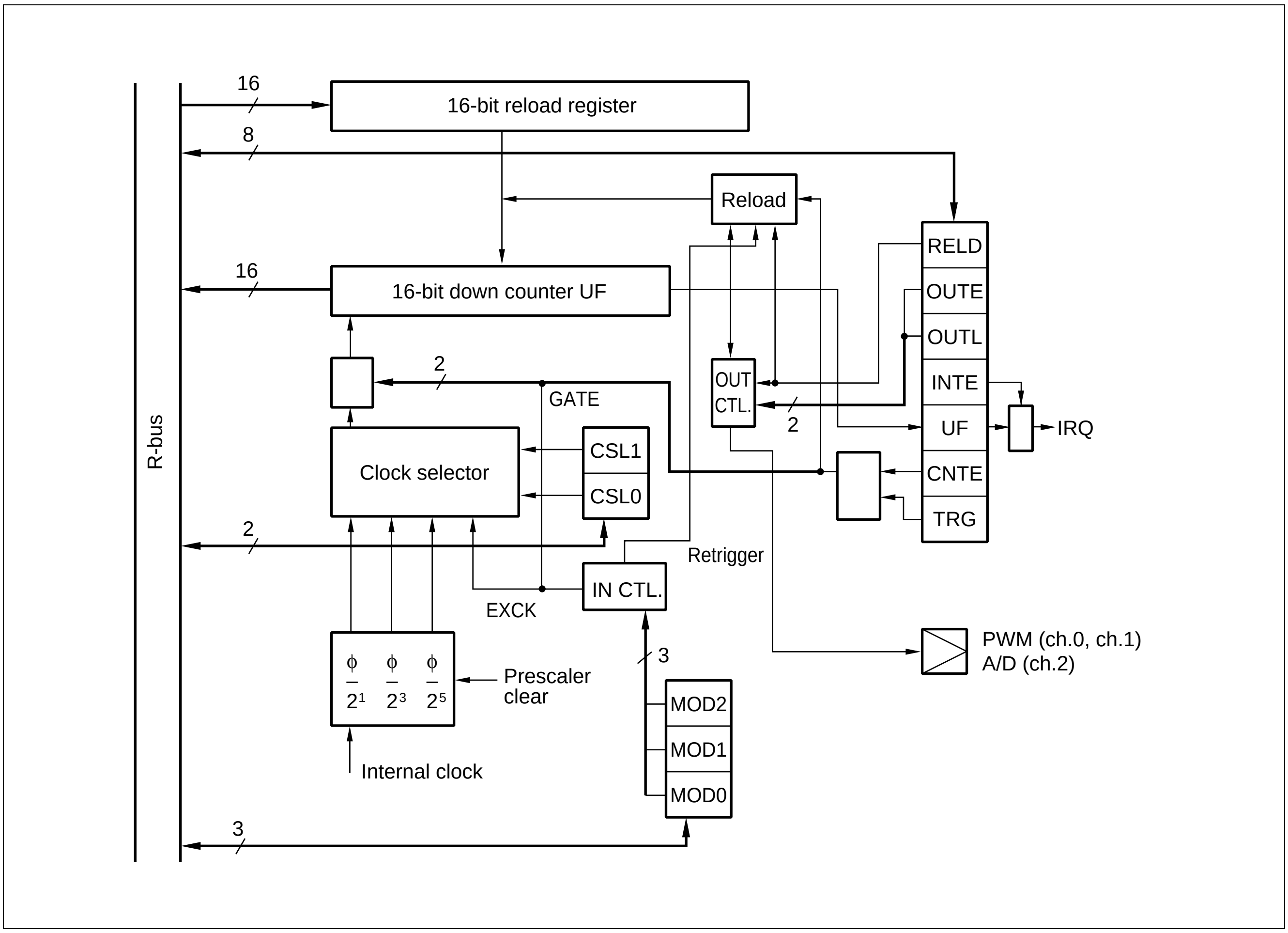
The 16-bit reload timer consists of a 16-bit down counter, a 16-bit reload timer, a prescaler for generating internal count clock and control registers.

Internal clock can be selected from 3 types of internal clocks (divided by 2/8/32 of machine clock).

The DMA transfer can be started by the interruption.

The MB91101 consists of 3 channels of the 16-bit reload timer.

- **Block diagram**



MB91101 Series

- **Register configuration**

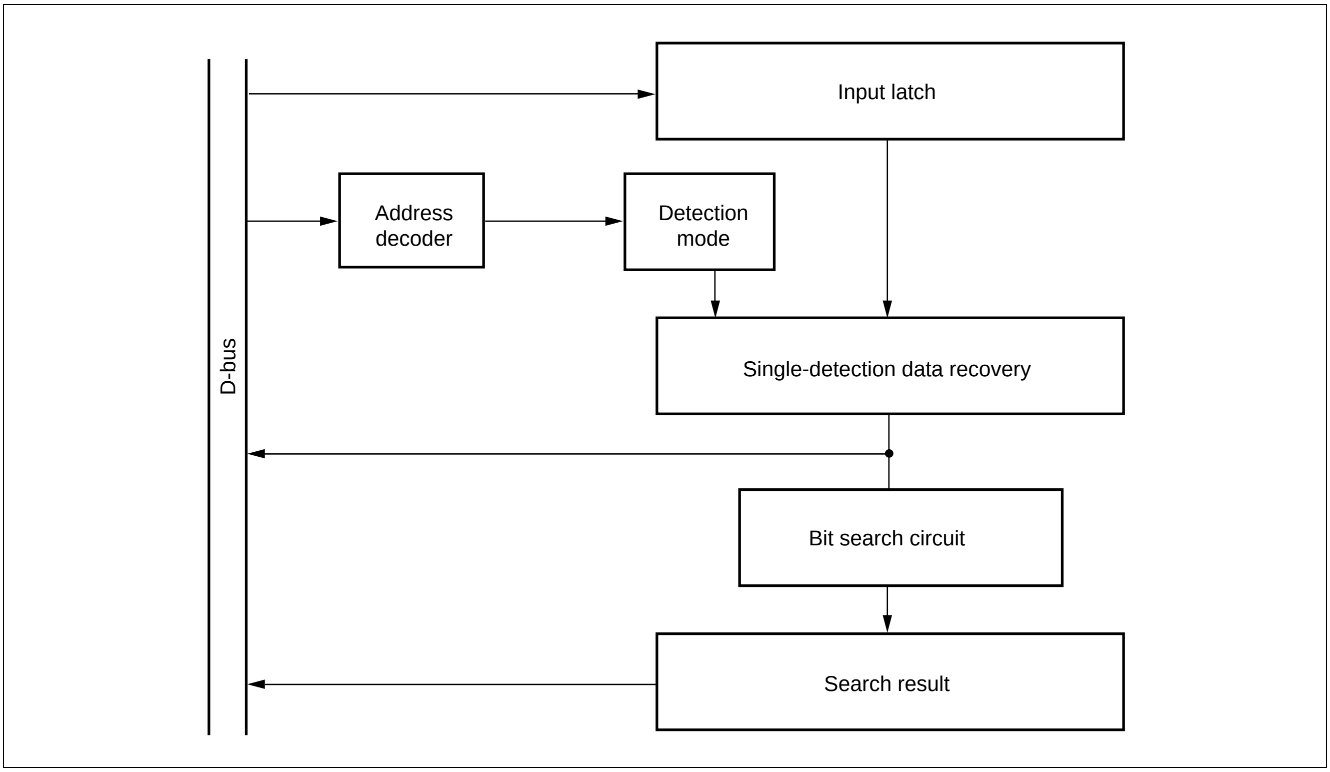
Address	bit 15 … bit 0	Initial value	Access
0000002EH 0000002FH	TMCSR0	- - - - 0 0 0 0 B 0 0 0 0 0 0 0 0 B	(R/W)
00000036H 00000037H	TMCSR1	- - - - 0 0 0 0 B 0 0 0 0 0 0 0 0 B	(R/W)
00000042H 00000043H	TMCSR2	- - - - 0 0 0 0 B 0 0 0 0 0 0 0 0 B	(R/W)
0000002AH 0000002BH	TMR0	X X X X X X X X B X X X X X X X X B	(R)
00000032H 00000033H	TMR1	X X X X X X X X B X X X X X X X X B	(R)
0000003EH 0000003FH	TMR2	X X X X X X X X B X X X X X X X X B	(R)
00000028H 00000029H	TMRLR0	X X X X X X X X B X X X X X X X X B	(W)
00000030H 00000031H	TMRLR1	X X X X X X X X B X X X X X X X X B	(W)
0000003CH 0000003DH	TMRLR2	X X X X X X X X B X X X X X X X X B	(W)

( ) : Access
R/W : Readable and writable
R : Read only
W : Write only
– : Unused
X : Indeterminate

7. Bit Search Module

The bit search module detects transitions of data (0 to 1/1 to 0) on the data written on the input registers and returns locations of the transitions.

- **Block diagram**



- **Register configuration**

Address	bit 31 … bit 16 … bit 0	Initial value	
000003F0H 000003F1H 000003F2H 000003F3H	BSD0	XXXXXXXXB XXXXXXXXB XXXXXXXXB XXXXXXXXB	(W)
000003F4H 000003F5H 000003F6H 000003F7H	BSD1	XXXXXXXXB XXXXXXXXB XXXXXXXXB XXXXXXXXB	(W)
000003F8H 000003F9H 000003FAH 000003FBH	BSDC	XXXXXXXXB XXXXXXXXB XXXXXXXXB XXXXXXXXB	(W)
000003FCH 000003FEH 000003FDH 000003FFH	BSRR	XXXXXXXXB XXXXXXXXB XXXXXXXXB XXXXXXXXB	(W)

( ) : Access
R/W : Readable and writable
R : Read only
W : Write only
X : Indeterminate

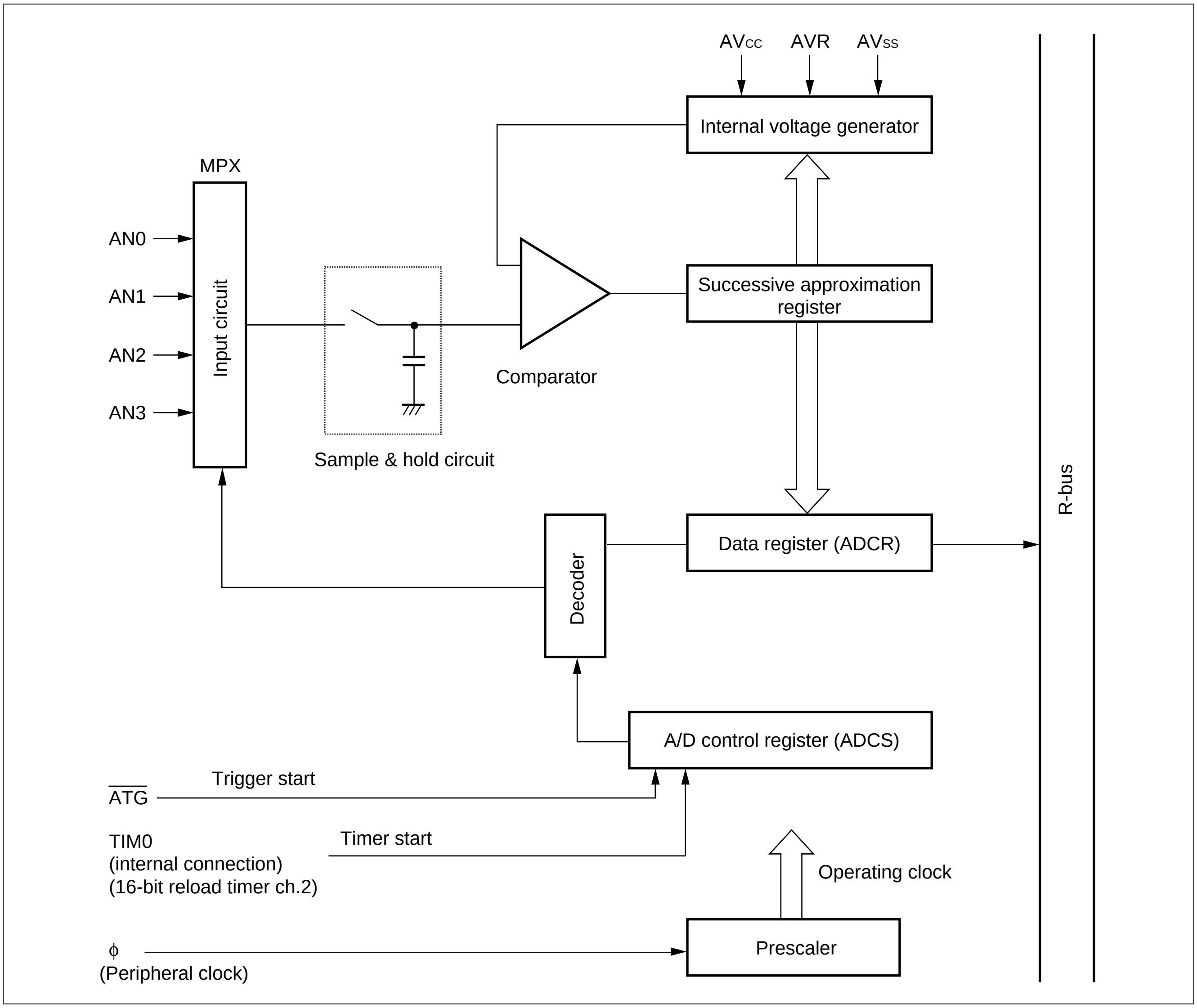
MB91101 Series

8. 10-bit A/D Converter (Successive Approximation Conversion Type)

The A/D converter is the module which converts an analog input voltage to a digital value, and it has following features.

- Minimum converting time: 5.6 µs/ch. (system clock: 25 MHz)
- Inner sample and hold circuit
- Resolution: 10 bits
- Analog input can be selected from 4 channels by program.
  Single convert mode: 1 channel is selected and converted.
  Scan convert mode: Converting continuous channels. Maximum 4 channels are programmable.
  Continuous convert mode: Converting the specified channel repeatedly.
  Stop convert mode: After converting one channel then stop and wait till next activation synchronising at the beginning of conversion can be peformed.
- DMA transfer operation is available by interruption.
- Operating factor can be selected from the software, the external trigger (falling edge), and 16-bit reroad timer (rising edge).

• Block diagram



- **Register configuration**

Address	bit 15 … bit 0	Initial value	
0000003AH 0000003BH	ADCS	0 0 0 0 0 0 0 0 B 0 0 0 0 0 0 0 0 B	(R/W)
00000038H 00000039H	ADCR	- - - - - - X X B X X X X X X X X B	(R)

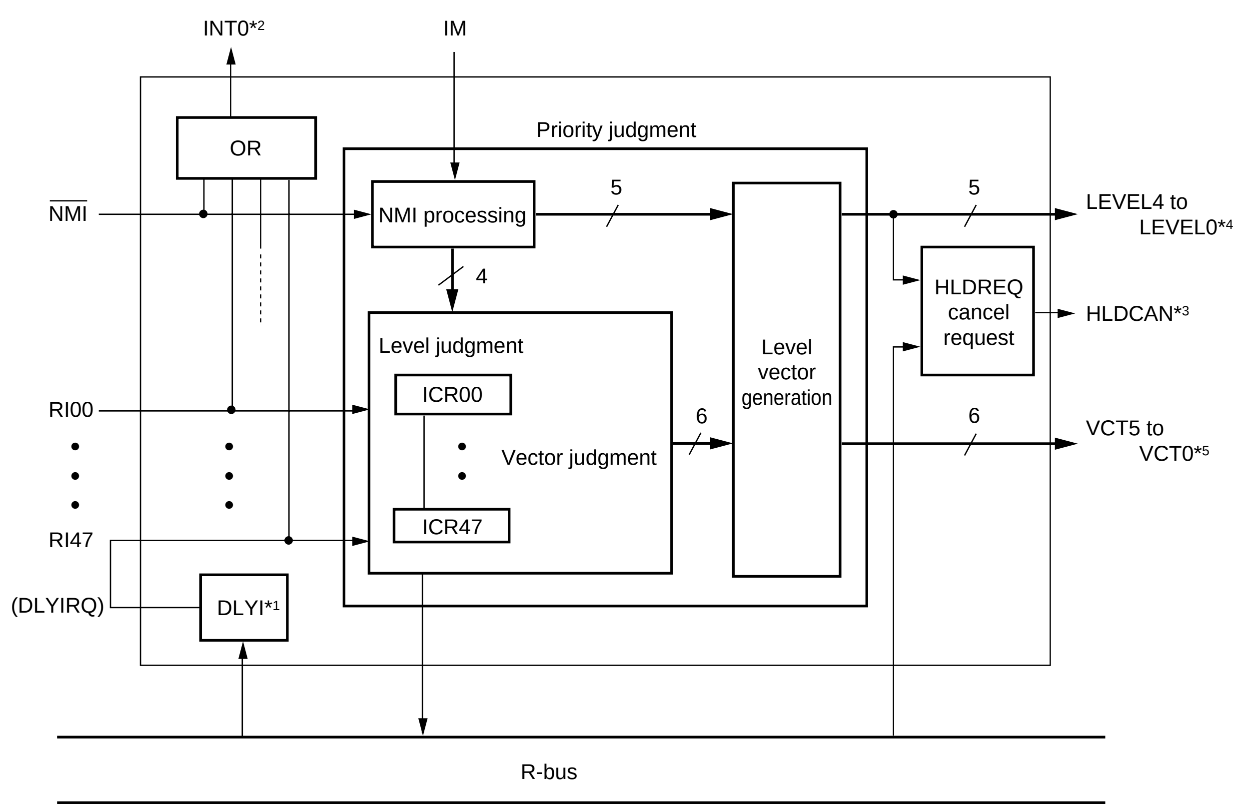
( ) : Access
R/W : Readable and writable
R : Read only
– : Unused
X : Indeterminate

MB91101 Series

9. Interrupt Controller

The interrupt controller processes interrupt acknowledgments and arbitration between interrupts.

- **Block diagram**



*1: DLYI stands for delayed interrupt module (delayed interrupt generation block) (refer to the section “11. Delayed Interrupt Module” for detail).

*2: INT0 is a wake-up signal to clock control block in the sleep or stop status.

*3: HLDCAN is a bus release request signal for bus masters other than CPU.

*4: LEVEL5 to LEVEL0 are interrupt level outputs.

*5: VCT5 to VCT0 are interrupt vector outputs.

- **Register configuration**

Address	bit 7 … bit 0	Initial value	Address	bit 7 … bit 0	Initial value
00000400H	ICR00	- - - 11111 B (R/W)	00000411H	ICR17	- - - 11111 B (R/W)
00000401H	ICR01	- - - 11111 B (R/W)	00000412H	ICR18	- - - 11111 B (R/W)
00000402H	ICR02	- - - 11111 B (R/W)	00000413H	ICR19	- - - 11111 B (R/W)
00000403H	ICR03	- - - 11111 B (R/W)	00000414H	ICR20	- - - 11111 B (R/W)
00000404H	ICR04	- - - 11111 B (R/W)	00000415H	ICR21	- - - 11111 B (R/W)
00000405H	ICR05	- - - 11111 B (R/W)	00000416H	ICR22	- - - 11111 B (R/W)
00000406H	ICR06	- - - 11111 B (R/W)	00000417H	ICR23	- - - 11111 B (R/W)
00000407H	ICR07	- - - 11111 B (R/W)	00000418H	ICR24	- - - 11111 B (R/W)
00000408H	ICR08	- - - 11111 B (R/W)	00000419H	ICR25	- - - 11111 B (R/W)
00000409H	ICR09	- - - 11111 B (R/W)	0000041AH	ICR26	- - - 11111 B (R/W)
0000040AH	ICR10	- - - 11111 B (R/W)	0000041BH	ICR27	- - - 11111 B (R/W)
0000040BH	ICR11	- - - 11111 B (R/W)	0000041CH	ICR28	- - - 11111 B (R/W)
0000040CH	ICR12	- - - 11111 B (R/W)	0000041DH	ICR29	- - - 11111 B (R/W)
0000040DH	ICR13	- - - 11111 B (R/W)	0000041EH	ICR30	- - - 11111 B (R/W)
0000040EH	ICR14	- - - 11111 B (R/W)	0000041FH	ICR31	- - - 11111 B (R/W)
0000040FH	ICR15	- - - 11111 B (R/W)	0000042FH	ICR47	- - - 11111 B (R/W)
00000410H	ICR16	- - - 11111 B (R/W)	00000431H	HRCL	- - - 11111 B (R/W)
			00000430H	DICR	- - - - - - - 0 B (R/W)

( ) : Access
R/W : Redable and writable
– : Unused

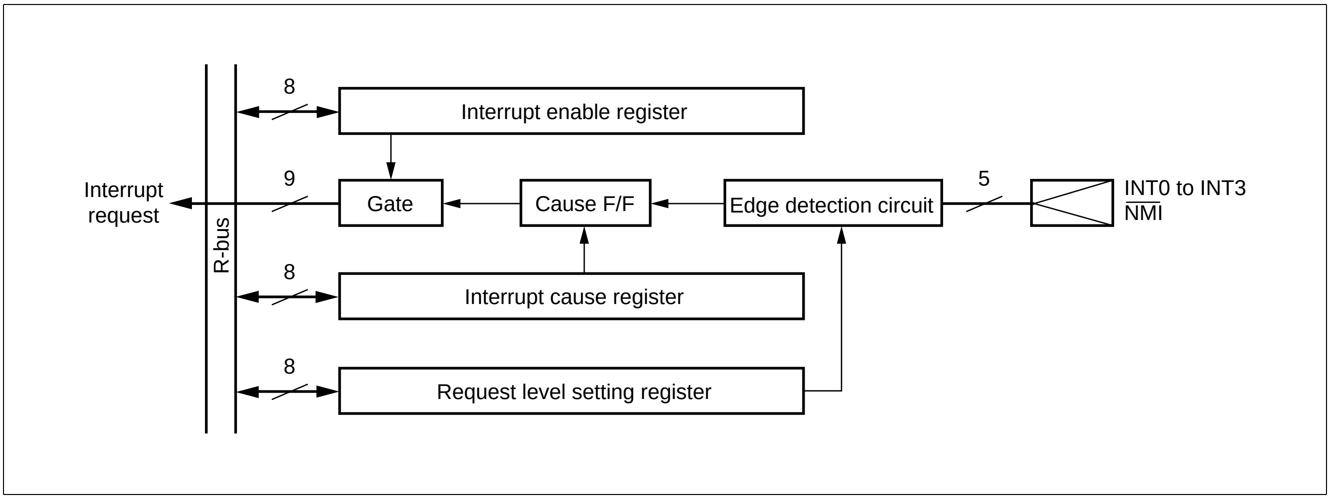
MB91101 Series

10. External Interrupt/NMI Control Block

The external interrupt/NMI control block controls external interrupt request signals input to NMI pin and INT0 to INT3 pins.

Detecting levels can be selected from “H”, “L”, rising edge and falling edge (not for NMI pin).

- **Block diagram**



- **Register configuration**

Address	bit 15	bit 8	bit 0	Initial value	
00000095H		ENIR		00000000 B	(R/W)
00000094H	EIRR			00000000 B	(R/W)
00000099H	ELVR			00000000 B	(R/W)

( ) : Access
R/W : Redable and writable

11. Delayed Interrupt Module

Delayed interrupt module is a module which generates a interrupt for changing a task. By using this delayed interrupt module, an interrupt request to CPU can be generated/cancelled by the software.

Refer to the section “9. Interrupt Controller” for delayed interrupt module block diagram.

- **Register configuration**

Address	bit 7 … bit 0	Initial value
00000430H	DICR	- - - - - - - 0 B (R/W)

( ) : Access
R/W : Redable and writable
– : Unused

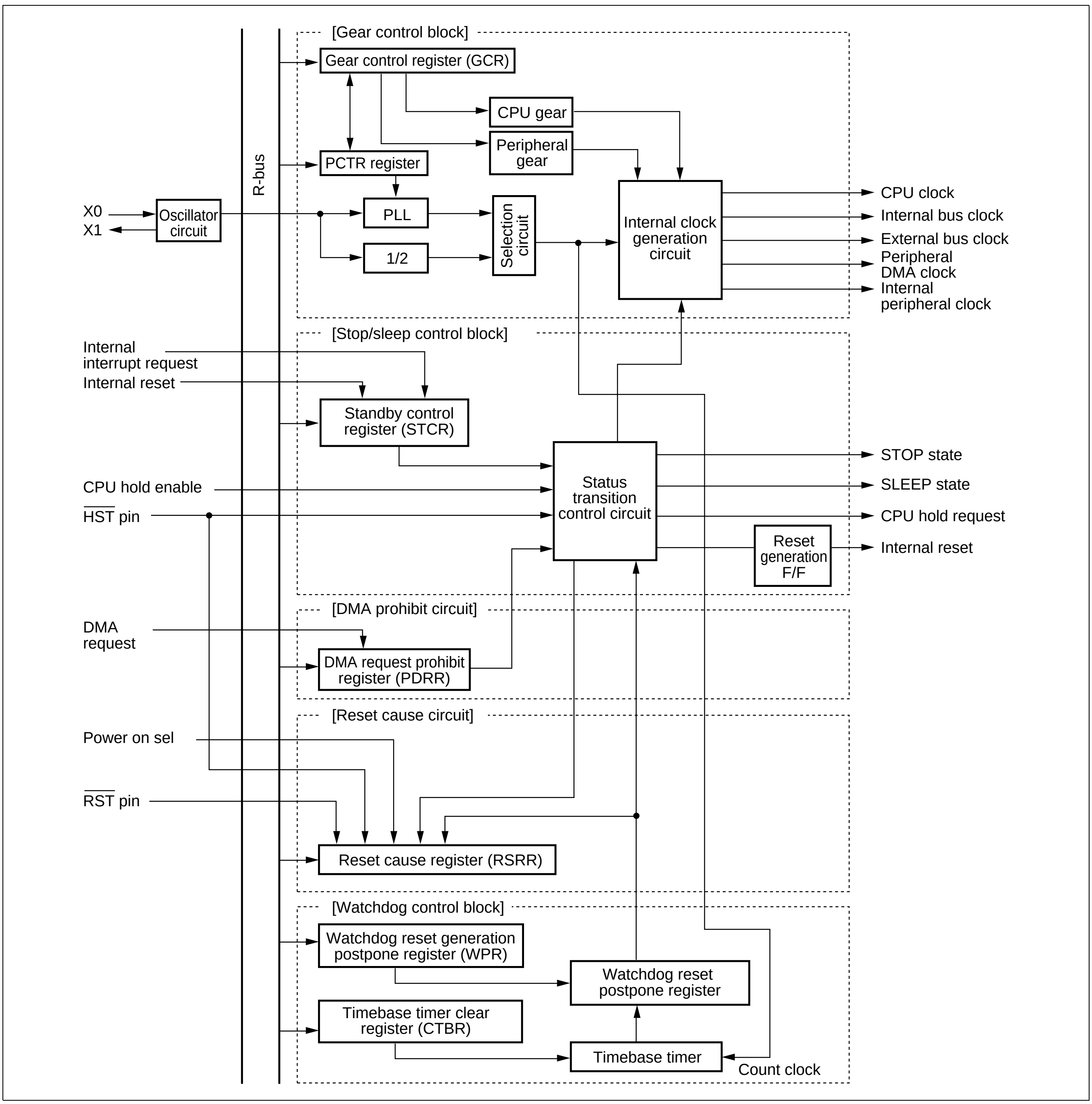
MB91101 Series

12. Clock Generation (Low-power consumption mechanism)

The clock control block is a module which undertakes the following functions.

- CPU clock generation (including gear function)
- Peripheral clock generation (including gear function)
- Reset generation and cause hold
- Standby function (including hardware standby)
- DMA request prohibit
- PLL (multiplier circuit) embedded

- **Block diagram**



- **Register configuration**

Address	bit 15 … bit 8	… bit 0	Initial value	
00000480$_H$	RSRR/WTCR		1 X X X X - 0 0 $_B$	(R/W)
00000481$_H$		STCR	0 0 0 1 1 1 - - $_B$	(R/W)
00000482$_H$	PDRR		- - - - 0 0 0 0 $_B$	(R/W)
00000483$_H$		CTBR	X X X X X X X X $_B$	(W)
00000484$_H$	GCR		1 1 0 0 1 1 - 1 $_B$	(R/W)
00000485$_H$		WPR	X X X X X X X X $_B$	(W)

( ) : Access
R/W : Redable and writable
W : Write only
– : Unused
X : Indeterminate

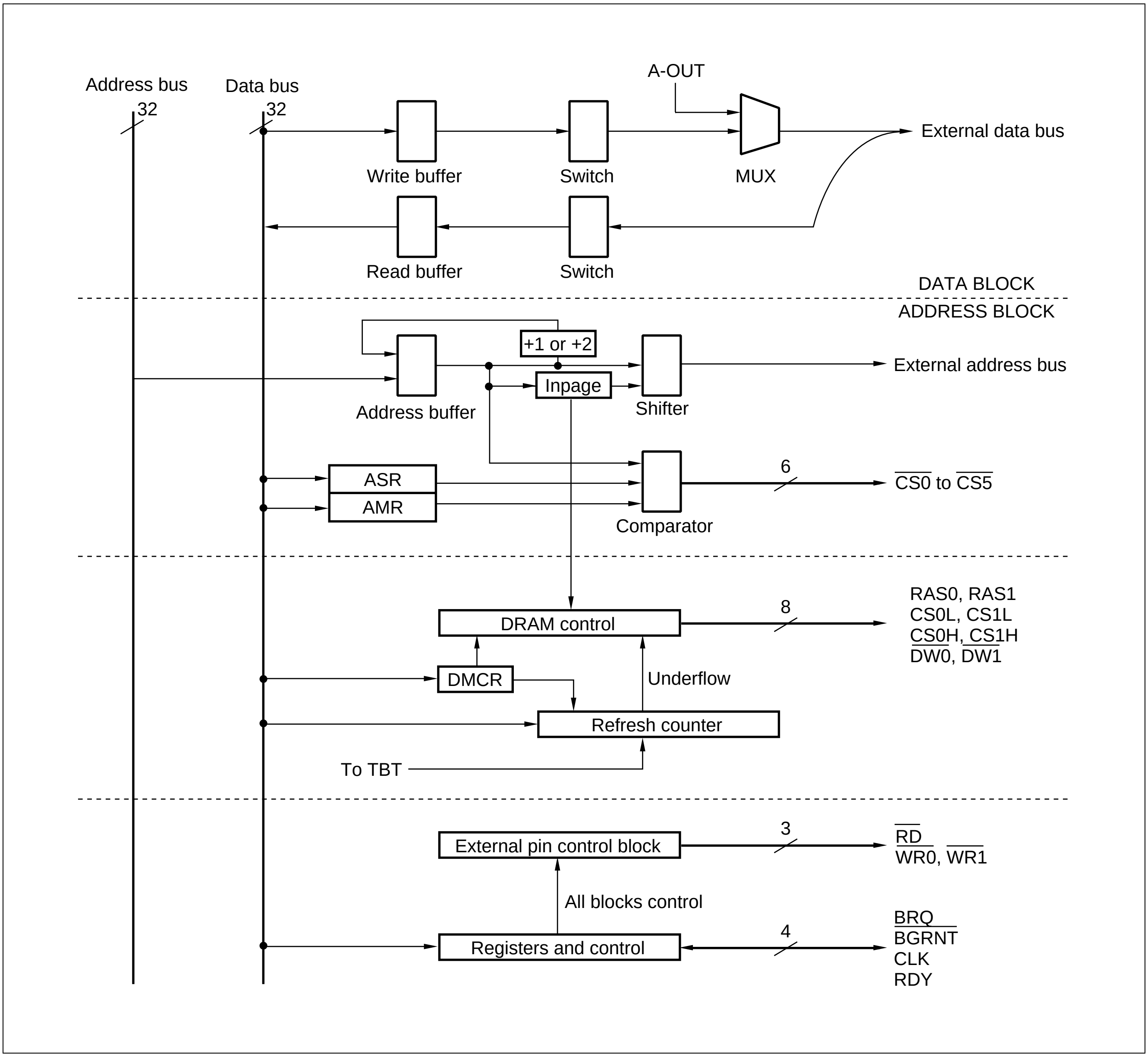
MB91101 Series

13. External Bus Interface

The external bus interface controls the interface between the device and the external memory and also the external I/O, and has the following features.

- 25-bit (32 Mbytes) address output
- 6 independent banks owing to the chip select function.
  Can be set to anywhere on the logical address space for minimum unit 64 Kbytes.
  Total 32 Mbytes × 6 area setting is available by the address pin and the chip select pin.
- 8/16-bit bus width setting are available for every chip select area.
- Programmable automatic memory wait (max. for 7 cycles) can be inserted.
- DRAM interface support
  Three kinds of DRAM interface: Double CAS DRAM (normally DRAM I/F)
  Single CAS DRAM
  Hyper DRAM
  2 banks independent control (RAS, CAS, etc. control signals)
  DRAM select is available from 2CAS/1WE and 1CAS/2WE.
  Hi-speed page mode supported
  CBR/self refresh supported
  Programmable wave form
- Unused address/data pin can be used for I/O port.
- Little endian mode supported
- Clock doublure: Internal bus 50 MHz, external bus 25 MHz

• **Block diagram**



- **Register configuration**

Address	bit 31 … bit 16	bit 16 … bit 0	Initial value	Access
0000060CH 0000060DH	ASR1		0 0 0 0 0 0 0 0 B 0 0 0 0 0 0 0 1 B	(W)
0000060EH 0000060FH		AMR1	0 0 0 0 0 0 0 0 B 0 0 0 0 0 0 0 0 B	(W)
00000610H 00000611H	ASR2		0 0 0 0 0 0 0 0 B 0 0 0 0 0 0 1 0 B	(W)
00000612H 00000613H		AMR2	0 0 0 0 0 0 0 0 B 0 0 0 0 0 0 0 0 B	(W)
00000614H 00000615H	ASR3		0 0 0 0 0 0 0 0 B 0 0 0 0 0 0 1 1 B	(W)
00000616H 00000617H		AMR3	0 0 0 0 0 0 0 0 B 0 0 0 0 0 0 0 0 B	(W)
00000618H 00000619H	ASR4		0 0 0 0 0 0 0 0 B 0 0 0 0 0 1 0 0 B	(W)
0000061AH 0000061BH		AMR4	0 0 0 0 0 0 0 0 B 0 0 0 0 0 0 0 0 B	(W)
0000061CH 0000061DH	ASR5		0 0 0 0 0 0 0 0 B 0 0 0 0 0 1 0 1 B	(W)
0000061EH 0000061FH		AMR5	0 0 0 0 0 0 0 0 B 0 0 0 0 0 0 0 0 B	(W)
00000620H	AMD0		- - - 0 0 1 1 1 B	(R/W)
00000621H	AMD1		0 - - 0 0 0 0 0 B	(R/W)
00000622H		AMD32	0 0 0 0 0 0 0 0 B	(R/W)
00000623H		AMD4	0 - - 0 0 0 0 0 B	(R/W)
00000624H	AMD5		0 - - 0 0 0 0 0 B	(R/W)
00000625H	DSCR		0 0 0 0 0 0 0 0 B	(W)
00000626H 00000627H		RFCR	- - X X X X X X B 0 0 - - - 0 0 0 B	(R/W)
00000628H 00000629H	EPCR0		- - - - 1 1 0 0 0 B - 1 1 1 1 1 1 1 B	(W)
0000062BH		EPCR1	1 1 1 1 1 1 1 1 B	(W)
0000062CH 0000062DH	DMCR4		0 0 0 0 0 0 0 0 B 0 0 0 0 0 0 0 - B	(R/W)
0000062EH 0000062FH		DMCR5	0 0 0 0 0 0 0 0 B 0 0 0 0 0 0 0 - B	(R/W)
000007FEH		LER	- - - - - 0 0 0 B	(W)
000007FFH		MODR	X X X X X X X X B	(W)

( ) : Access
R/W : Redable and writable
W : Write only
– : Unused
X : Indeterminate

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

(V_{SS} = AV_{SS} = 0.0 V)

Parameter		Symbol	Value		Unit	Remarks
			Min.	Max.		
Power supply voltage	At 5 V power supply	$V_{CC}5$	V_{SS} – 0.3	V_{SS} + 6.5	V	
		$V_{CC}3$	—	—	V	
	At 3 V power supply	$V_{CC}5$	$V_{CC}3$ – 0.3	V_{SS} + 6.5	V	*1
		$V_{CC}3$	V_{SS} – 0.3	V_{SS} + 3.6	V	*1
Analog supply voltage		AV_{CC}	V_{SS} – 0.3	V_{SS} + 3.6	V	*2
Analog reference voltage		AVRH	V_{SS} – 0.3	V_{SS} + 3.6	V	*2
Analog pin input voltage		V_{IA}	V_{SS} – 0.3	AV_{CC} + 0.3	V	
Input voltage		V_I	V_{SS} – 0.3	$V_{CC}5$ + 0.3	V	
Output voltage		V_O	V_{SS} – 0.3	$V_{CC}5$ + 0.3	V	
"L" level maximum output current		I_{OL}	—	10	mA	*3
"L" level average output current		I_{OLAV}	—	4	mA	*4
"L" level maximum total output current		ΣI_{OL}	—	100	mA	
"L" level average total output current		ΣI_{OLAV}	—	50	mA	*5
"H" level maximum output current		I_{OH}	—	–10	mA	*3
"H" level average output current		I_{OHAV}	—	–4	mA	*4
"H" level maximum total output current		ΣI_{OH}	—	–50	mA	
"H" level average total output current		ΣI_{OHAV}	—	–20	mA	*5
Power consumption		P_D	—	500	mW	
Operating temperature		T_A	0	+70	°C	
Storage temperature		Tstg	–55	+150	°C	

*1: $V_{CC}5$ must not be less than V_{SS} – 0.3 V.
*2: Make sure that the voltage does not exceed $V_{CC}5$ + 0.3 V, such as when turning on the device.
*3: Maximum output current is a peak current value measured at a corresponding pin.
*4: Average output current is an average current for a 100 ms period at a corresponding pin.
*5: Average total output current is an average current for a 100 ms period for all corresponding pins.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

(1) At 5 V operation (4.5 V to 5.5 V)

(V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	$V_{CC}5$	4.5	5.5	V	Normal operation *1
	$V_{CC}5$	*1	*1	V	Retaining the RAM state in stop mode
	$V_{CC}3$	—	—	V	*2
Analog supply voltage	AV_{CC}	V_{SS} + 2.7	V_{CC} + 3.6	V	
Analog reference voltage	AVRH	V_{SS} – 0.3	AV_{CC}	V	
Operating temperature	T_A	0	+70	°C	
Smoothing capacitor	C_S	0.1	1.0	µF	$V_{CC}3$ pin *2

*1: At $V_{CC}5$, the RAM state holding is not warranted in stop mode.
*2: $V_{CC}3$ is used for the bypass capacitor pin.
*3: Use the ceramic capacitor or the capacitor whose frequency characteristic is equivalent to that of the ceramic capacitor.
And select the larger capacity smoothing condenser to connect to the power supply ($V_{CC}5$) than C_S.

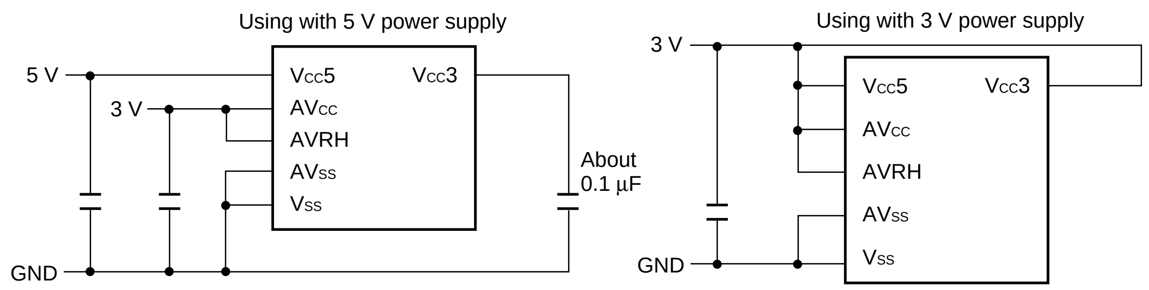
(2) At 3 V operation (2.7 V to 3.6 V)

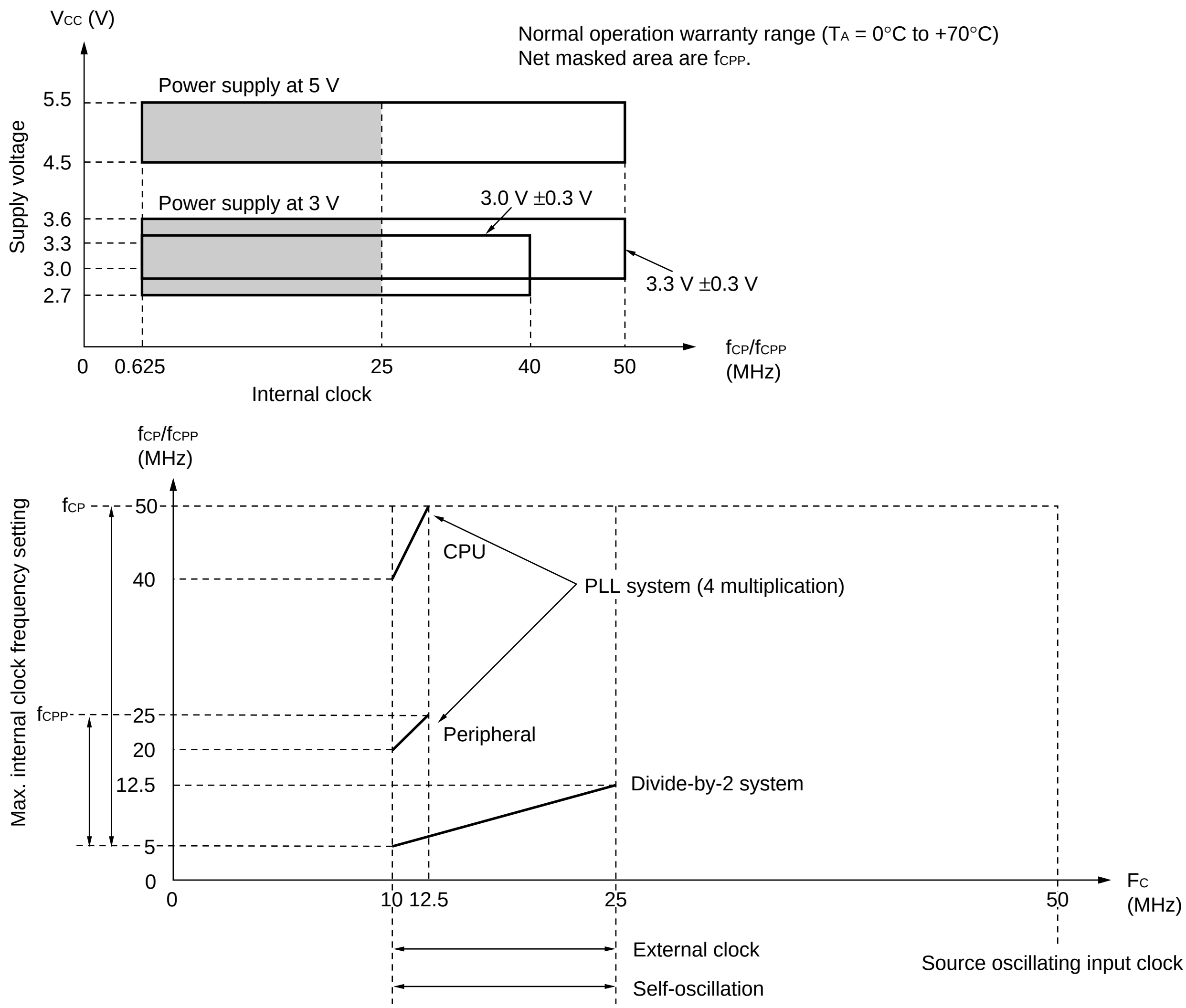
(V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	$V_{CC}5$	2.7	3.6	V	Normal operation
	$V_{CC}5$	2.7	3.6	V	Retaining the RAM state in stop mode
	$V_{CC}3$	2.7	3.6	V	*
Analog power supply voltage	AV_{CC}	V_{SS} + 2.7	V_{CC} + 3.6	V	
Analog reference voltage	AVRH	AV_{SS}	AV_{CC}	V	
Operating temperature	T_A	0	+70	°C	

* : Connect to $V_{CC}5$ for the power supply pin.

- **Connecting to a power supply**





Notes:
- When using PLL, the external clock must be used between 10.0 MHz to 12.5 MHz.
- PLL oscillation stabilizing period > 100 µs
- The setting of internal clock must be within above ranges.

WARNING: Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

3. DC Characteristics

($V_{CC}5$ = 5.0 V ±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = 0°C to +70°C)
($V_{CC}5$ = $V_{CC}3$ = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, T_A = 0°C to +70°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
"H" level input voltage	V_{IH}	Input pin except for hysteresis input	—	0.65 × $V_{CC}3$	—	$V_{CC}5$ + 0.3	V	*
	V_{IHS}	$\overline{HST}$, $\overline{NMI}$, $\overline{RST}$, PA1 to PA6, PB0 to PB7, PE0 to PE7, PF0 to PF7	—	0.8 × $V_{CC}3$	—	$V_{CC}5$ + 0.3	V	Hysteresis input *
"L" level input voltage	V_{IL}	Input other than following symbols	—	V_{SS} – 0.3	—	0.25 × $V_{CC}3$	V	*
	V_{ILS}	$\overline{HST}$, $\overline{NMI}$, $\overline{RST}$, PA1 to PA6, PB0 to PB7, PE0 to PE7, PF0 to PF7	—	V_{SS} – 0.3	—	0.2 × $V_{CC}3$	V	Hysteresis input *
"H" level output voltage	V_{OH}	D16 to D31, A00 to A24, P6 to PF	$V_{CC}5$ = 4.5 V, I_{OH} = –4.0 mA	V_{CC} – 0.5	—	—	V	
"L" level output voltage	V_{OL}	D16 to D31, A00 to A24, P6 to PF	$V_{CC}5$ = 4.5 V, I_{OL} = 4.0 mA	—	—	0.4	V	
Input leakage current (Hi-Z output leakage current)	I_{LI}	D00 to D31, A00 to A23, P8 to PF	$V_{CC}5$ = 5.5 V, 0.45 V < V_I < V_{CC}	–5	—	+5	µA	
Pull-up resistance	R_{PULL}	$\overline{RST}$	$V_{CC}5$ = 5.5 V, V_I = 0.45 V	25	50	100	kΩ	
Power supply current	I_{CC}	V_{CC}	F_C = 12.5 MHz, $V_{CC}5$ = 5.5 V	—	75	100	mA	(4 multiplication) Operation at 50 MHz
	I_{CCS}	V_{CC}	F_C = 12.5 MHz, $V_{CC}5$ = 5.5 V	—	40	60	mA	Sleep mode
	I_{CCH}	V_{CC}	T_A = +25°C, $V_{CC}5$ = 5.5 V	—	10	100	µA	Stop mode
Input capacitance	C_{IN}	Except for $V_{CC}5$, $V_{CC}3$, AV_{CC}, AV_{SS}, V_{SS}	—	—	10	—	pF	

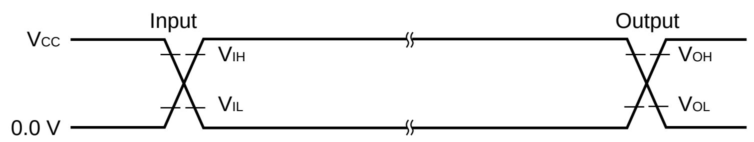
* : $V_{CC}3$ = 3.3 ±0.2 V (internal regulator output voltage) when using 5 V power supply, $V_{CC}3$ = power supply voltage when using 3 V power supply (internal regulator unused)

4. AC Characteristics

(1) Measurement Conditions

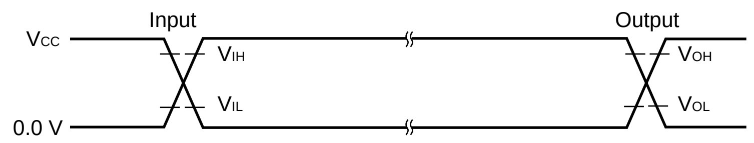
• **V_{CC} = 5.0 V ±10%**

Parameter	Symbol	Value			Unit	Remarks
		Min.	Typ.	Max.		
"H" level input voltage	V_{IH}	—	2.4	—	V	
"L" level input voltage	V_{IL}	—	0.8	—	V	
"H" level output voltage	V_{OH}	—	2.4	—	V	
"L" level output voltage	V_{OL}	—	0.8	—	V	



• **V_{CC} = 2.7 V to 3.6 V**

Parameter	Symbol	Value			Unit	Remarks
		Min.	Typ.	Max.		
"H" level input voltage	V_{IH}	—	1/2 × V_{CC}	—	V	
"L" level input voltage	V_{IL}	—	1/2 × V_{CC}	—	V	
"H" level output voltage	V_{OH}	—	1/2 × V_{CC}	—	V	
"L" level output voltage	V_{OL}	—	1/2 × V_{CC}	—	V	



MB91101 Series

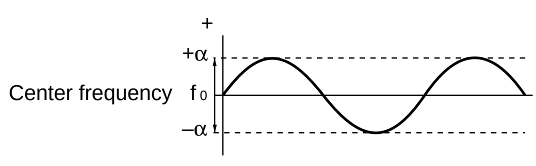
(2) Clock Timing Rating

($V_{CC}5$ = 5.0 V ±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = 0°C to +70°C)
($V_{CC}5$ = $V_{CC}3$ = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, T_A = 0°C to +70°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Clock frequency	F_C	X0, X1	When using PLL	10	12.5	MHz	
	F_C	X0, X1	Self-oscillation (divide-by-2 input)	10	25	MHz	
	F_C	X0, X1	External clock (divide-by-2 input)	10	25	MHz	
Clock cycle time	t_C	X0, X1	When using PLL	80	100	ns	
	t_C	X0, X1	—	40	100	ns	
Frequency shift ratio (when locked)	Δf	—	When using PLL	—	5	%	*1
Input clock pulse width	P_{WH}, P_{WL}	X0, X1	—	25	—	ns	Input to X0 only, when using 5 V power supply
	P_{WH}, P_{WL}	X0, X1		10	—	ns	Input to X0, X1
Input clock rising/falling time	t_{CR}, t_{CF}	X0, X1		—	8	ns	(t_{CR} + t_{CF})
Internal operating clock frequency	f_{CP}	—	CPU system	0.625*2	50	MHz	
	f_{CPB}	—	Bus system	0.625*2	25*3	MHz	
	f_{CPP}	—	Peripheral system	0.625*2	25	MHz	
Internal operating clock cycle time	t_{CP}	—	CPU system	20	1600*2	ns	
	t_{CPB}	—	Bus system	40*3	1600*2	ns	
	t_{CPP}	—	Peripheral system	40	1600*2	ns	

*1: Frequency shift ratio stands for deviation ratio of the operating clock from the center frequency in the clock multiplication system.

$$\Delta f = \frac{|\alpha|}{f_0} \times 100\ (\%)$$

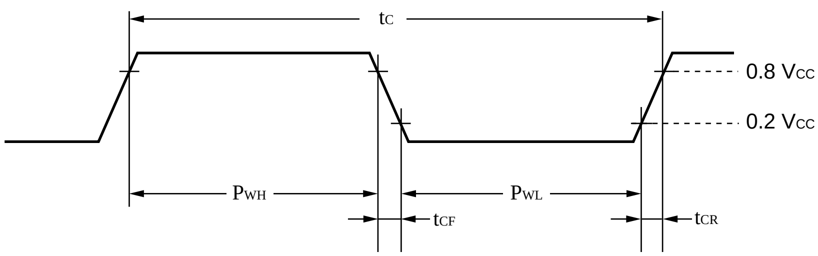


*2: These values are for a minimum clock of 10 MHz input to X0, a divide-by-2 system of the source oscillation and a 1/8 gear.

*3: Values when using the doublure and CPU operation at 50 MHz.

- **Load conditions**

- **Clock timing rating measurement conditions**



MB91101 Series

(3) Clock Output Timing

($V_{CC}5$ = 5.0 V ±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = 0°C to +70°C)
($V_{CC}5$ = $V_{CC}3$ = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, T_A = 0°C to +70°C)

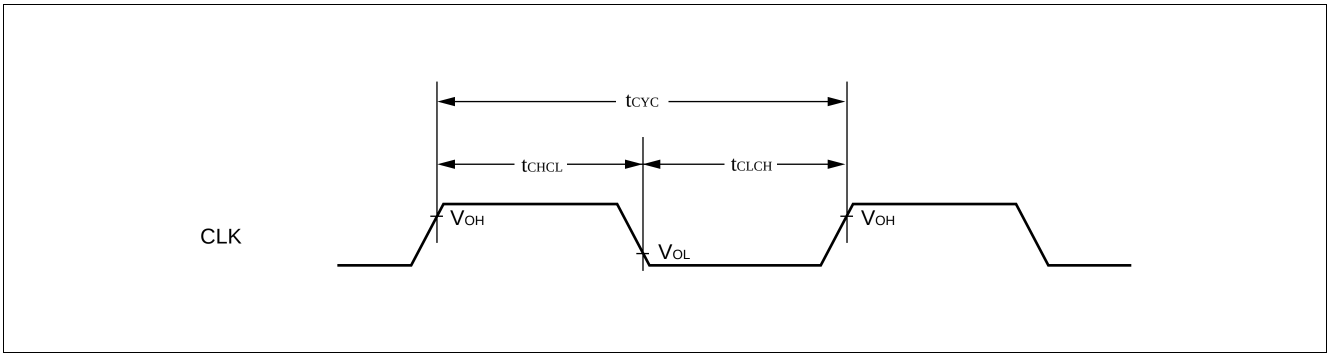
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Cycle time	t_{CYC}	CLK	—	t_{CP}	—	ns	*1
	t_{CYC}	CLK	Using the doublure	t_{CPB}	—	ns	
CLK ↑ → CLK ↓	t_{CHCL}	CLK	—	1/2 × t_{CYC} – 10	1/2 × t_{CYC} + 10	ns	*2
CLK ↓ → CLK ↑	t_{CLCH}	CLK		1/2 × t_{CYC} – 10	1/2 × t_{CYC} + 10	ns	*3

t_{CP}, t_{CPB} (internal operating clock cycle time): Refer to "(2) Clock Timing Rating."

*1: t_{CYC} is a frequency for 1 clock cycle including a gear cycle.
Use the doublure when CPU frequency is above 25 MHz.

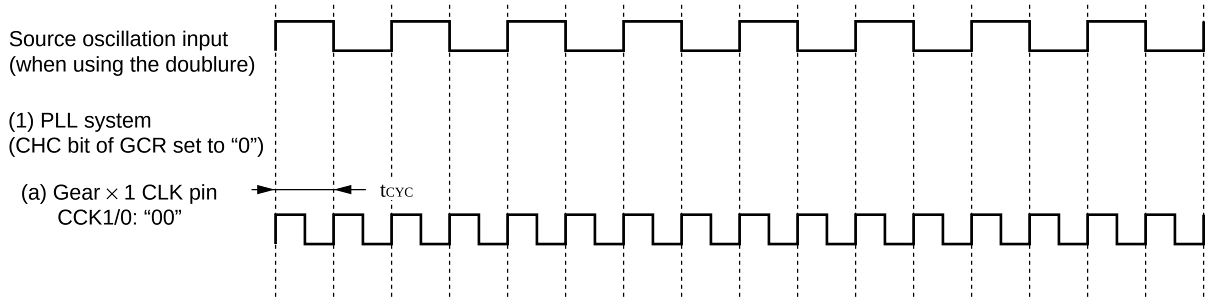
*2: Rating at a gear cycle of × 1.
When a gear cycle of 1/2, 1/4, 1/8 is selected, substitute "n" in the following equations with 1/2, 1/4, 1/8, respectively.
Min. : (1 – n/2) × t_{CYC} – 10
Max. : (1 – n/2) × t_{CYC} + 10
Select a gear cycle of × 1 when using the doublure.

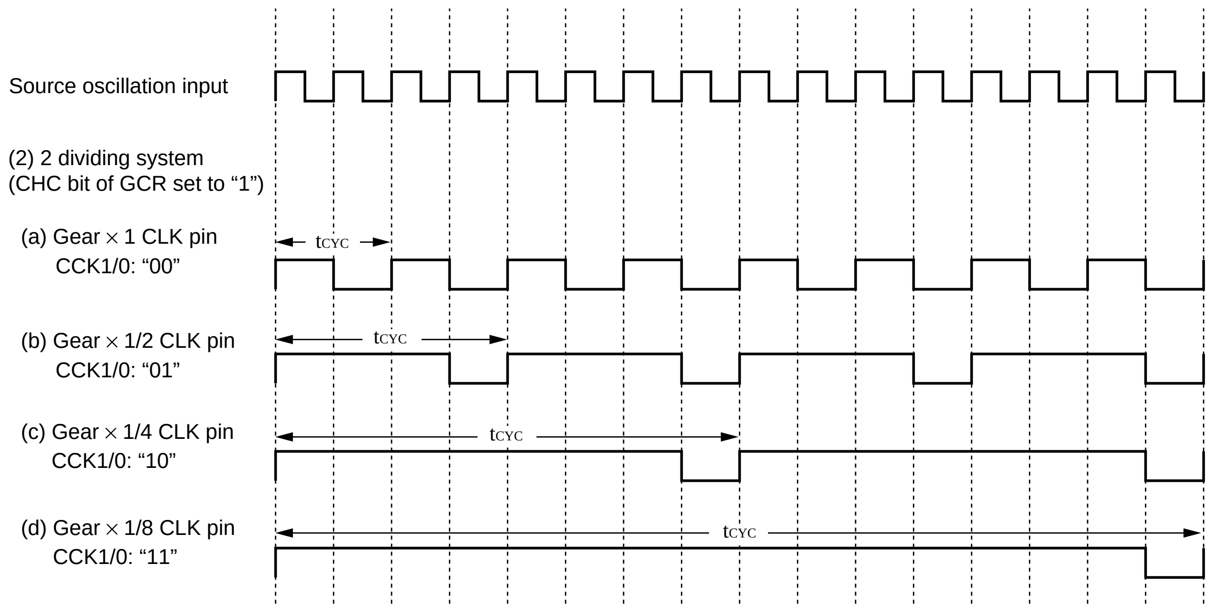
*3: Rating at a gear cycle of × 1.
When a gear cycle of 1/2, 1/4, 1/8 is selected, substitute "n" in the following equations with 1/2, 1/4, 1/8, respectively.
Min. : n/2 × t_{CYC} – 10
Max. : n/2 × t_{CYC} + 10
Select a gear cycle of × 1 when using the doublure.



The relation between source oscillation input and CLK pin for configured by CHC/CCK1/CCK0 settings of GCR (gear control register) is as follows:

However, in this chart source oscillation input means X0 input clock.

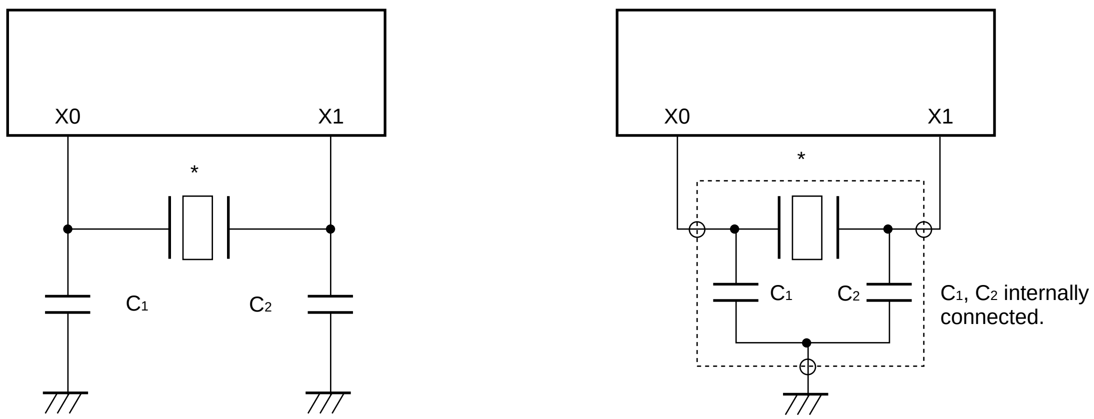




MB91101 Series

- **Ceramic oscillator applications**

Recommended circuit (2 contacts) Recommended circuit (3 contacts)



* : Murata Mfg. Co., Ltd.

- **Discreet type**

Oscillation frequency [MHz]	Model	Load capacitance $C_1 = C_2$ [pF]	Power supply voltage $V_{CC}5$ [V]
5.00 to 6.30	CSA□□□MG	30	2.9 to 5.5
	CST□□□MGW	(30)	
	CSA□□□MG093	30	2.7 to 5.5
	CST□□□MGW093	(30)	
6.31 to 10.0	CSA□□□MTZ	30	2.9 to 5.5
	CST□□□MTW	(30)	
	CSA□□□MTZ093	30	2.7 to 5.5
	CST□□□MTW093	(30)	
10.1 to 13.0	CSA□□□MTZ	30	3.0 to 5.5
	CST□□□MTW	(30)	
	CSA□□□MTZ093	30	2.9 to 5.5
	CST□□□MTW093	(30)	
13.01 to 15.00	CSA□□□□MXZ040	15	3.2 to 5.5
	CST□□□□MXW0C3	(15)	

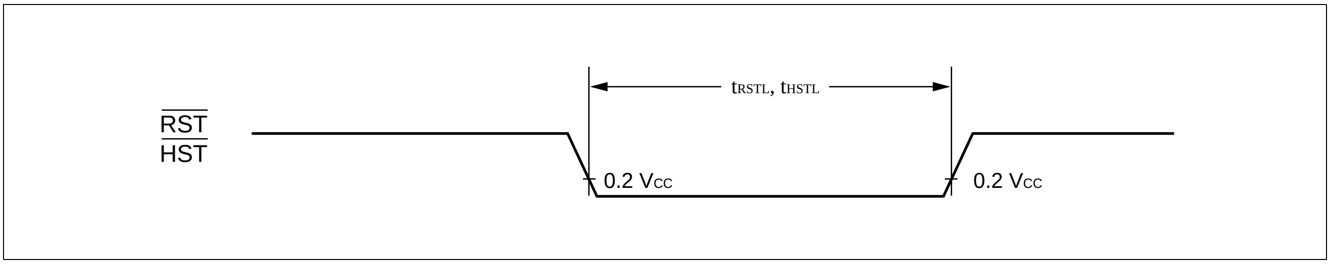
( ): C_1 and C_2 internally connected 3 contacts type.

(4) Reset/Hardware Standby Input Ratings

($V_{CC}5$ = 5.0 V ±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = 0°C to +70°C)
($V_{CC}5$ = $V_{CC}3$ = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, T_A = 0°C to +70°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Reset input time	t_{RSTL}	$\overline{RST}$	—	$t_{CP} \times 5$	—	ns	
Hardware standby input time	t_{HSTL}	$\overline{HST}$		$t_{CP} \times 5$	—	ns	

t_{CP} (internal operating clock cycle time): Refer to “(2) Clock Timing Rating.”



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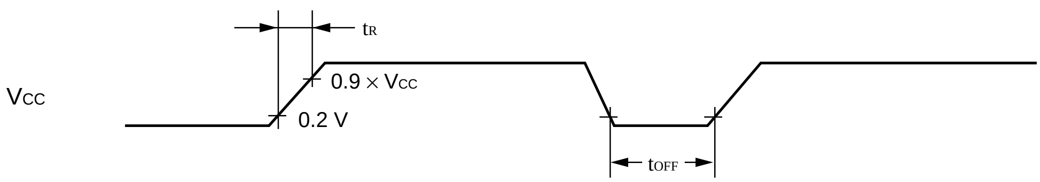
(5) Power on Supply Specifications (Power-on Reset)

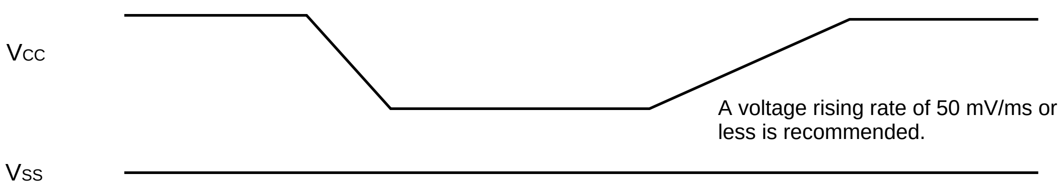
($V_{CC}5$ = 5.0 V ±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = 0°C to +70°C)
($V_{CC}5$ = $V_{CC}3$ = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, T_A = 0°C to +70°C)

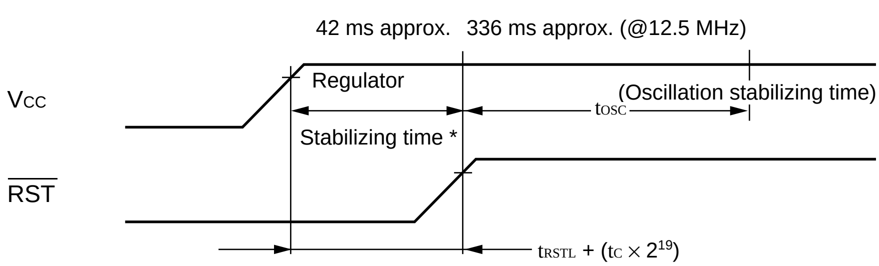
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Power supply rising time	t_R	V_{CC}	V_{CC} = 5.0 V	50	—	µs	*
	t_R	V_{CC}		—	30	ms	*
	t_R	V_{CC}	V_{CC} = 3.0/ 3.3 V	50	—	µs	*
	t_R	V_{CC}		—	18	ms	*
Power supply shut off time	t_{OFF}	V_{CC}	—	1	—	ms	Repeated operations
Oscillation stabilizing time	t_{OSC}	—		$2 \times t_C \times 2^{21}$ + 100 µs	—	ns	

t_C (clock cycle time): Refer to "(2) Clock Timing Rating."
* : V_{CC} < 0.2 V before the power supply rising



Note: Sudden change in supply voltage during operation may initiate a power-on sequence.
To change supply voltage during operation, it is recommended to smoothly raise the voltage to avoid rapid fluctuations in the supply voltage.





t_{RSTL}: Reset input time

*: Reset can't be done during regulator stabilizing time.

Note: Set $\overline{RST}$ pin to "L" level when turning on the device, at least the described above duration after the supply voltage reaches Vcc is necessary before turning the $\overline{RST}$ to "H" level.

(6) Normal Bus Access Read/write Operation

($V_{CC}5$ = 5.0 V ±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = 0°C to +70°C)
($V_{CC}5$ = $V_{CC}3$ = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, T_A = 0°C to +70°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
$\overline{CS0}$ to $\overline{CS5}$ delay time	t_{CHCSL}	CLK, $\overline{CS0}$ to $\overline{CS5}$	—	—	15	ns	
	t_{CHCSH}	CLK, $\overline{CS0}$ to $\overline{CS5}$		—	15	ns	
Address delay time	t_{CHAV}	CLK, A24 to A00		—	15	ns	
Data delay time	t_{CHDV}	CLK, D31 to D16		—	15	ns	
$\overline{RD}$ delay time	t_{CLRL}	CLK, $\overline{RD}$		—	6	ns	
	t_{CLRH}	CLK, $\overline{RD}$		—	6	ns	
$\overline{WR0}$, $\overline{WR1}$ delay time	t_{CLWL}	CLK, $\overline{WR0}$, $\overline{WR1}$		—	6	ns	
	t_{CLWH}	CLK, $\overline{WR0}$, $\overline{WR1}$		—	6	ns	
Valid address → valid data input time	t_{AVDV}	A24 to A00, D31 to D16		—	3/2 × t_{CYC} – 25	ns	*1 *2
$\overline{RD}$ ↓→ valid data input time	t_{RLDV}	$\overline{RD}$, D31 to D16		—	t_{CYC} – 10	ns	*1
Data set up → $\overline{RD}$ ↑ time	t_{DSRH}	$\overline{RD}$, D31 to D16		10	—	ns	
$\overline{RD}$ ↑→ data hold time	t_{RHDX}	$\overline{RD}$, D31 to D16		0	—	ns	

t_{CYC} (a cycle time of peripheral system clock): Refer to “(3) Clock Output Timing.”

*1: When bus timing is delayed by automatic wait insertion or RDY input, add (t_{CYC} × extended cycle number for delay) to this rating.

*2: Rating at a gear cycle of × 1.
When a gear cycle of 1/2, 1/4, 1/8 is selected, substitute “n” in the following equation with 1/2, 1/4, 1/8, respectively.
Equation: (2 – n/2) × t_{CYC} – 25

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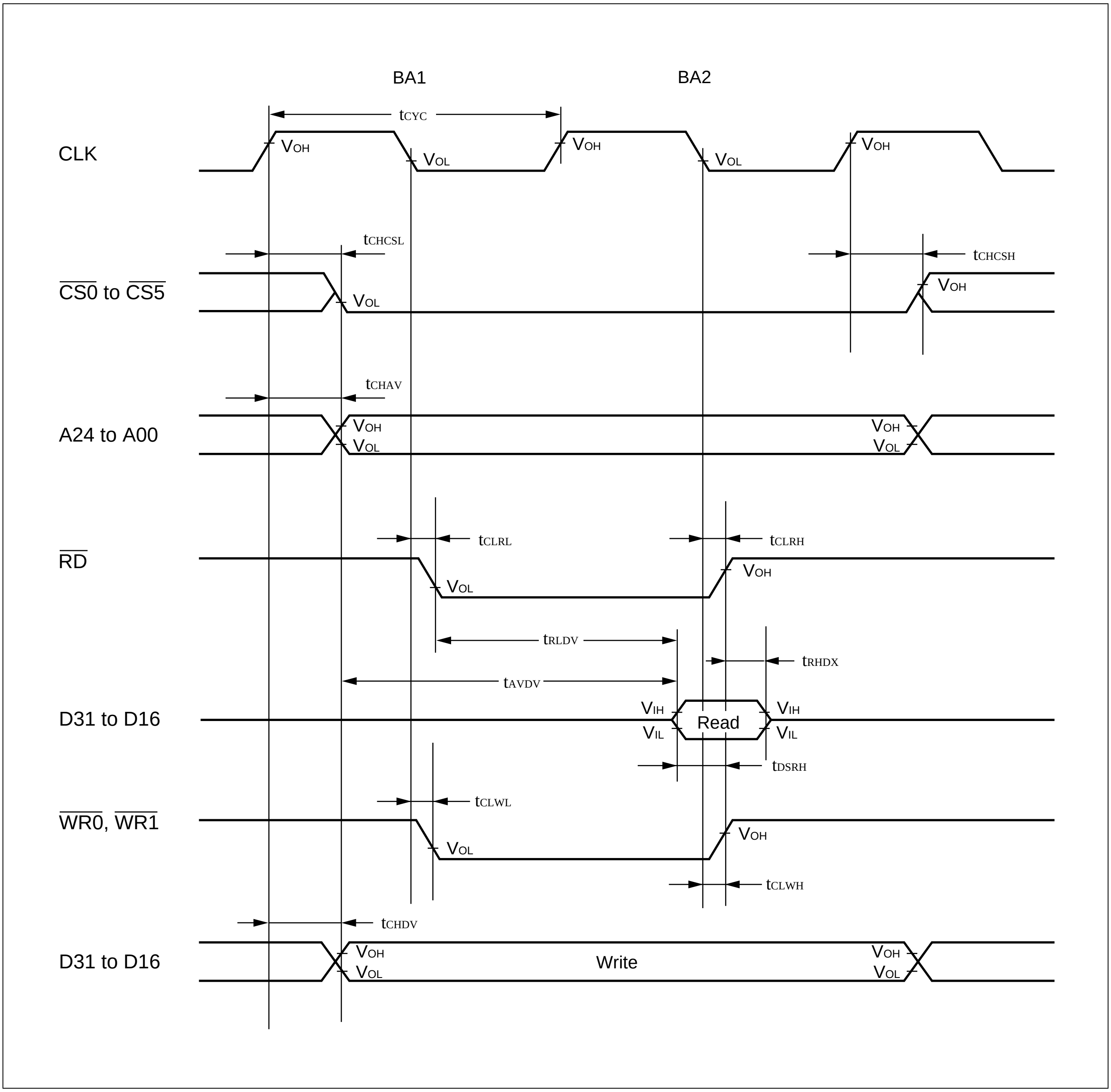
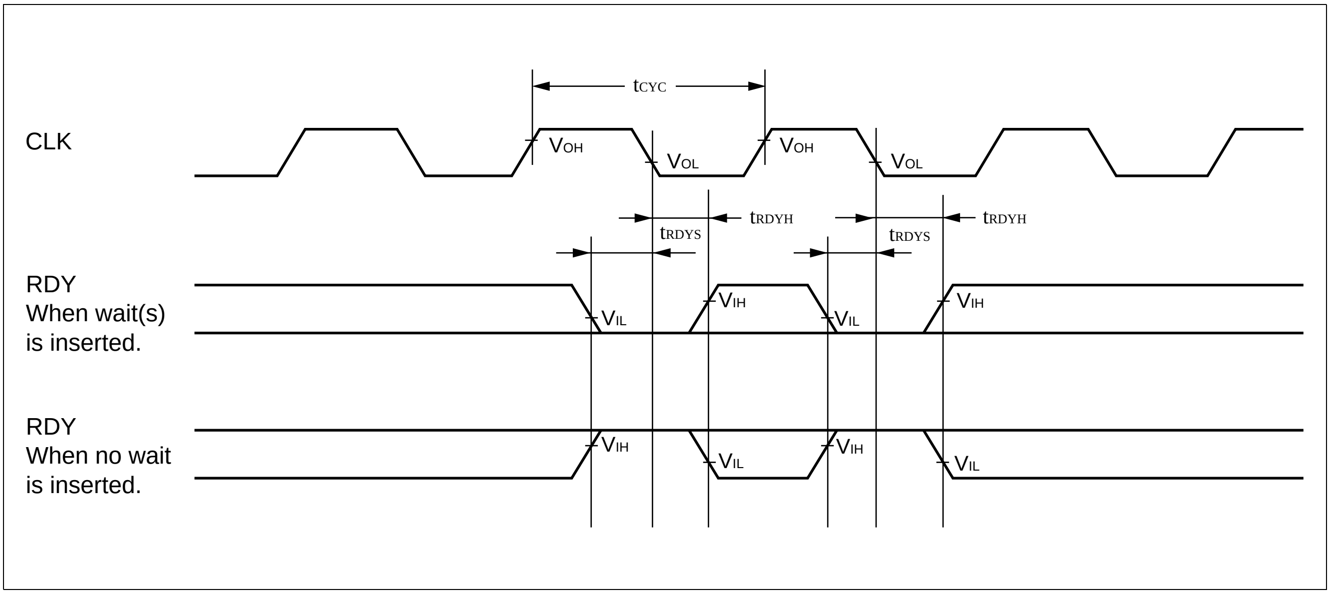


(7) Ready Input Timing

($V_{CC}5$ = 5.0 V ±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = 0°C to +70°C)
($V_{CC}5$ = $V_{CC}3$ = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, T_A = 0°C to +70°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
RDY set up time → CLK ↓	t_{RDYS}	RDY, CLK	—	15	—	ns	
CLK ↓→ RDY hold time	t_{RDYH}	CLK, RDY		0	—	ns	



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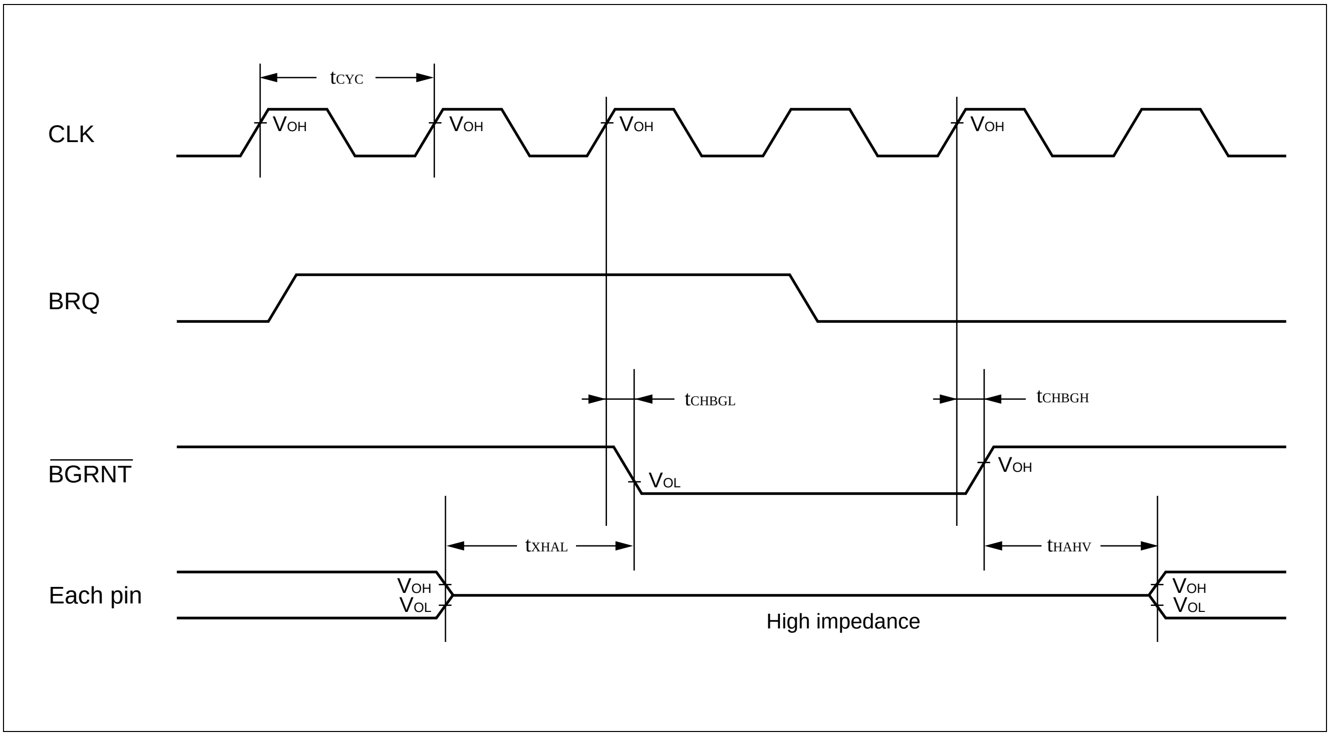
(8) Hold Timing

($V_{CC}5$ = 5.0 V ±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = 0°C to +70°C)
($V_{CC}5$ = $V_{CC}3$ = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, T_A = 0°C to +70°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
$\overline{\text{BGRNT}}$ delay time	t_{CHBGL}	CLK, $\overline{\text{BGRNT}}$	—	—	6	ns	
	t_{CHBGH}	CLK, $\overline{\text{BGRNT}}$		—	6	ns	
Pin floating → $\overline{\text{BGRNT}}$ ↓ time	t_{XHAL}	$\overline{\text{BGRNT}}$		t_{CYC} – 10	t_{CYC} + 10	ns	
$\overline{\text{BGRNT}}$ ↑→ pin valid time	t_{HAHV}	$\overline{\text{BGRNT}}$		t_{CYC} – 10	t_{CYC} + 10	ns	

t_{CYC} (a cycle time of peripheral system clock): Refer to “(3) Clock Output Timing.”

Note: There is a delay time of more than 1 cycle from BRQ input to $\overline{\text{BGRNT}}$ change.



(9) Normal DRAM Mode Read/Write Cycle

($V_{CC}5$ = 5.0 V ±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = 0°C to +70°C)
($V_{CC}5$ = $V_{CC}3$ = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, T_A = 0°C to +70°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
RAS delay time	t_{CLRAH}	CLK, RAS	—	—	6	ns	
	t_{CHRAL}	CLK, RAS		—	6	ns	
CAS delay time	t_{CLCASL}	CLK, CAS		—	6	ns	
	t_{CLCASH}	CLK, CAS		—	6	ns	
ROW address delay time	t_{CHRAV}	CLK, A24 to A00		—	15	ns	
COLUMN address delay time	t_{CHCAV}	CLK, A24 to A00		—	15	ns	
$\overline{DW}$ delay time	t_{CHDWL}	CLK, $\overline{DW}$		—	15	ns	
	t_{CHDWH}	CLK, $\overline{DW}$		—	15	ns	
Output data delay time	t_{CHDV1}	CLK, D31 to D16		—	15	ns	
RAS ↓→ valid data input time	t_{RLDV}	RAS, D31 to D16		—	5/2 × t_{CYC} – 16	ns	*1 *2
CAS ↓→ valid data input time	t_{CLDV}	CAS, D31 to D16		—	t_{CYC} – 17	ns	*1
CAS ↑→ data hold time	t_{CADH}	CAS, D31 to D16		0	—	ns	

t_{CYC} (a cycle time of peripheral system clock): Refer to “(3) Clock Output Timing.”

CAS: CS0L to CS1H pins are for CAS signal outputs.
$\overline{DW}$: $\overline{DW0}$, $\overline{DW1}$ and CS0H to CS1H are used for $\overline{WE}$ outputs.

*1: When Q1 cycle or Q4 cycle is extended for 1 cycle, add t_{CYC} time to this rating.
*2: Rating at a gear cycle of × 1.
When a gear cycle of 1/2, 1/4, 1/8 is selected, substitute “n” in the following equation with 1/2, 1/4, 1/8, respectively.
Equation: $(3 – n/2) \times t_{CYC} – 16$

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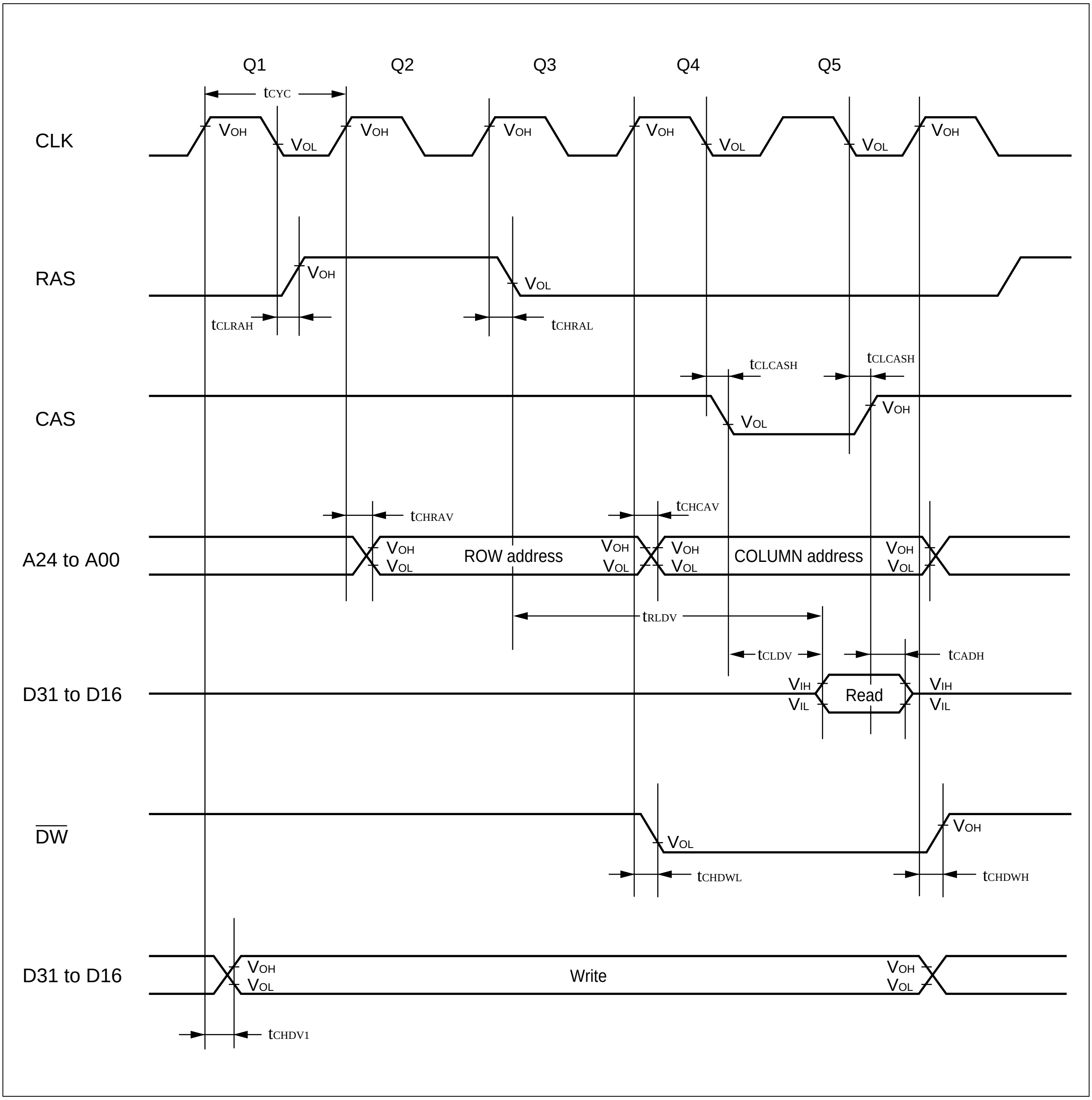

(10) **Normal DRAM Mode Fast Page Read/Write Cycle**

($V_{CC}5$ = 5.0 V ±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = 0°C to +70°C)
($V_{CC}5$ = $V_{CC}3$ = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, T_A = 0°C to +70°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
RAS delay time	t_{CLRAH}	CLK, RAS	—	—	6	ns	
CAS delay time	t_{CLCASL}	CLK, CAS		—	6	ns	
	t_{CLCASH}	CLK, CAS		—	6	ns	
COLUMN address delay time	t_{CHCAV}	CLK, A24 to A00		—	15	ns	
$\overline{DW}$ delay time	t_{CHDWH}	CLK, $\overline{DW}$		—	15	ns	
Output data delay time	t_{CHDV1}	CLK, D31 to D16		—	15	ns	
CAS ↓→ valid data input time	t_{CLDV}	CAS, D31 to D16		—	t_{CYC} – 17	ns	*
CAS ↑→ data hold time	t_{CADH}	CAS, D31 to D16		0	—	ns	

t_{CYC} (a cycle time of peripheral system clock): Refer to “(3) Clock Output Timing.”

CAS: CS0L to CS1H pins are for CAS signal outputs.
$\overline{DW}$: $\overline{DW0}$, $\overline{DW1}$ and CS0H to CS1H are used for $\overline{WE}$ outputs.

* : When Q4 cycle is extended for 1 cycle, add t_{CYC} time to this rating.

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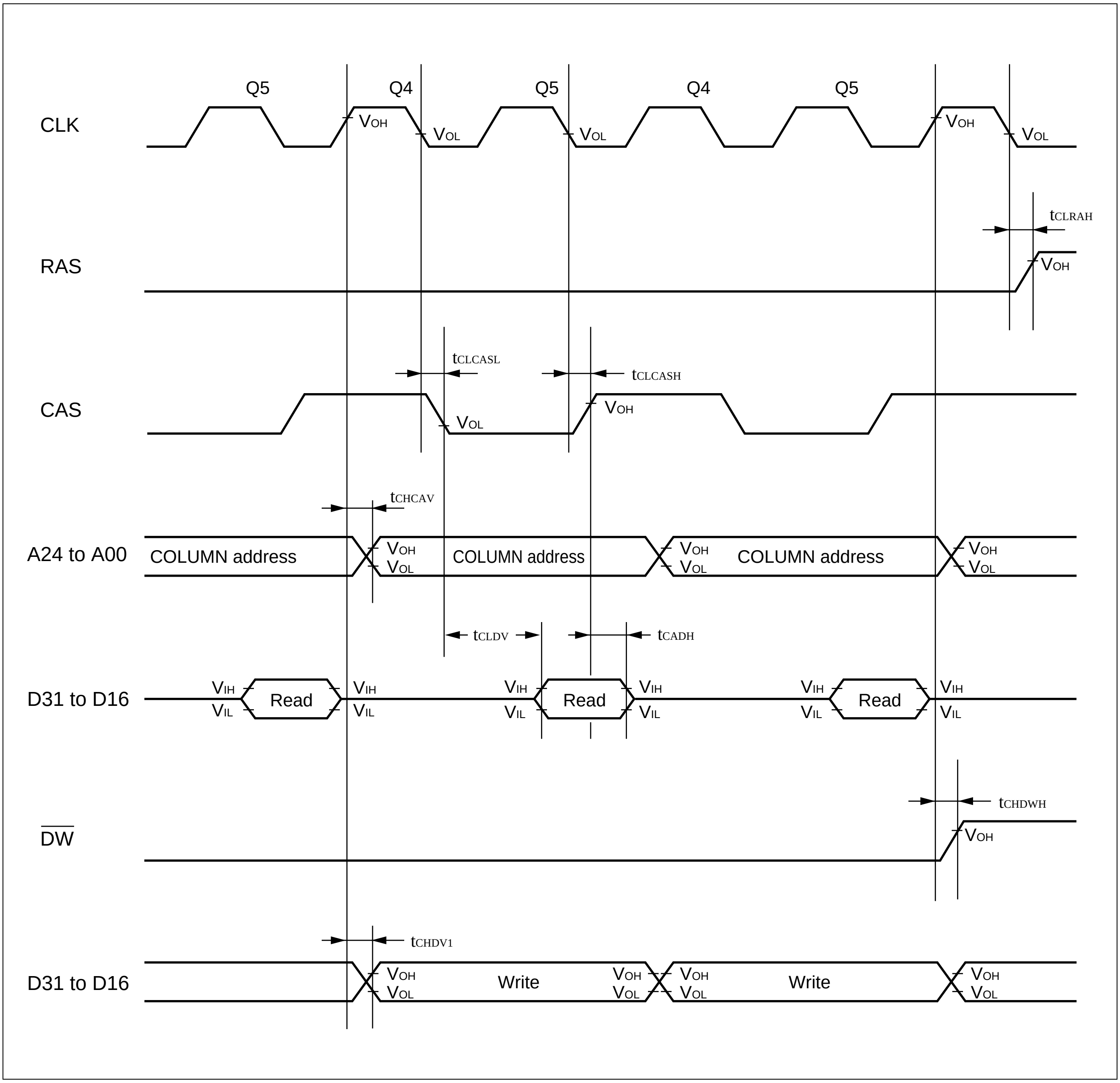


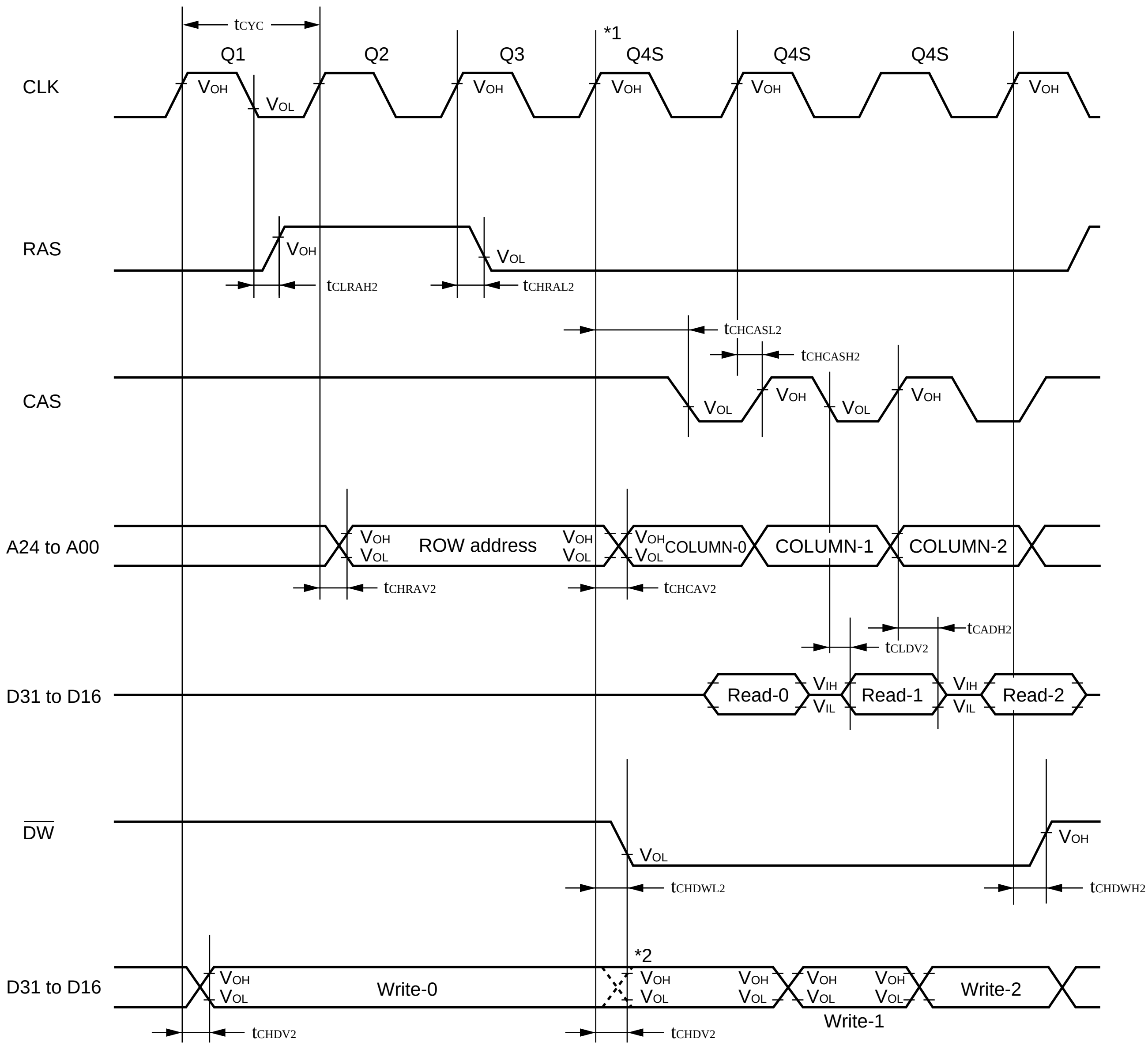
(11) Single DRAM Timing

($V_{CC}5 = 5.0$ V ±10%, $V_{SS} = AV_{SS} = 0.0$ V, $T_A = 0°C$ to +70°C)
($V_{CC}5 = V_{CC}3 = 2.7$ V to 3.6 V, $V_{SS} = AV_{SS} = 0.0$ V, $T_A = 0°C$ to +70°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
RAS delay time	t_{CLRAH2}	CLK, RAS	—	—	6	ns	
	t_{CHRAL2}	CLK, RAS			6	ns	
CAS delay time	$t_{CHCASL2}$	CLK, CAS		—	n/2 × t_{CYC}	ns	
	$t_{CHCASH2}$	CLK, CAS		—	6	ns	
ROW address delay time	t_{CHRAV2}	CLK, A24 to A00		—	15	ns	
COLUMN address delay time	t_{CHCAV2}	CLK, A24 to A00		—	15	ns	
$\overline{DW}$ delay time	t_{CHDWL2}	CLK, $\overline{DW}$		—	15	ns	
	t_{CHDWH2}	CLK, $\overline{DW}$		—	15	ns	
Output data delay time	t_{CHDV2}	CLK, D31 to D16		—	15	ns	
CAS ↓→ Valid data input time	t_{CLDV2}	CAS, D31 to D16		—	(1 – n/2) × t_{CYC} – 17	ns	
CAS ↑→ data hold time	t_{CADH2}	CLK, D31 to D16		0	—	ns	

t_{CYC} (a cycle time of peripheral system clock): Refer to "(3) Clock Output Timing."

MB91101 Series



*1: Q4S indicates Q4SR (Read) of Single DRAM cycle or Q4SW (Write) cycle.
*2: - - - - indicates the timing when the bus cycle begins from the high spead page mode.

(12) Hyper DRAM Timing

($V_{CC}5$ = 5.0 V ±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = 0°C to +70°C)
($V_{CC}5$ = $V_{CC}3$ = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, T_A = 0°C to +70°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
RAS delay time	t_{CLRAH3}	CLK, RAS	—	—	6	ns	
	t_{CHRAL3}	CLK, RAS		—	6	ns	
CAS delay time	$t_{CHCASL3}$	CLK, CAS		—	n/2 × t_{CYC}	ns	
	$t_{CHCASH3}$	CLK, CAS		—	6	ns	
ROW address delay time	t_{CHRAV3}	CLK, A24 to A00		—	15	ns	
COLUMN address delay time	t_{CHCAV3}	CLK, A24 to A00		—	15	ns	
$\overline{RD}$ delay time	t_{CHRL3}	CLK, $\overline{RD}$		—	15	ns	
	t_{CHRH3}	CLK, $\overline{RD}$		—	15	ns	
	t_{CLRL3}	CLK, $\overline{RD}$		—	15	ns	
$\overline{DW}$ delay time	t_{CHDWL3}	CLK, $\overline{DW}$		—	15	ns	
	t_{CHDWH3}	CLK, $\overline{DW}$		—	15	ns	
Output data delay time	t_{CHDV3}	CLK, D31 to D16		—	15	ns	
CAS ↓→ valid data input time	t_{CLDV3}	CAS, D31 to D16		—	t_{CYC} – 17	ns	
CAS ↓→ data hold time	t_{CADH3}	CLK, D31 to D16		0	—	ns	

t_{CYC} (a cycle time of peripheral system clock): Refer to “(3) Clock Output Timing.”

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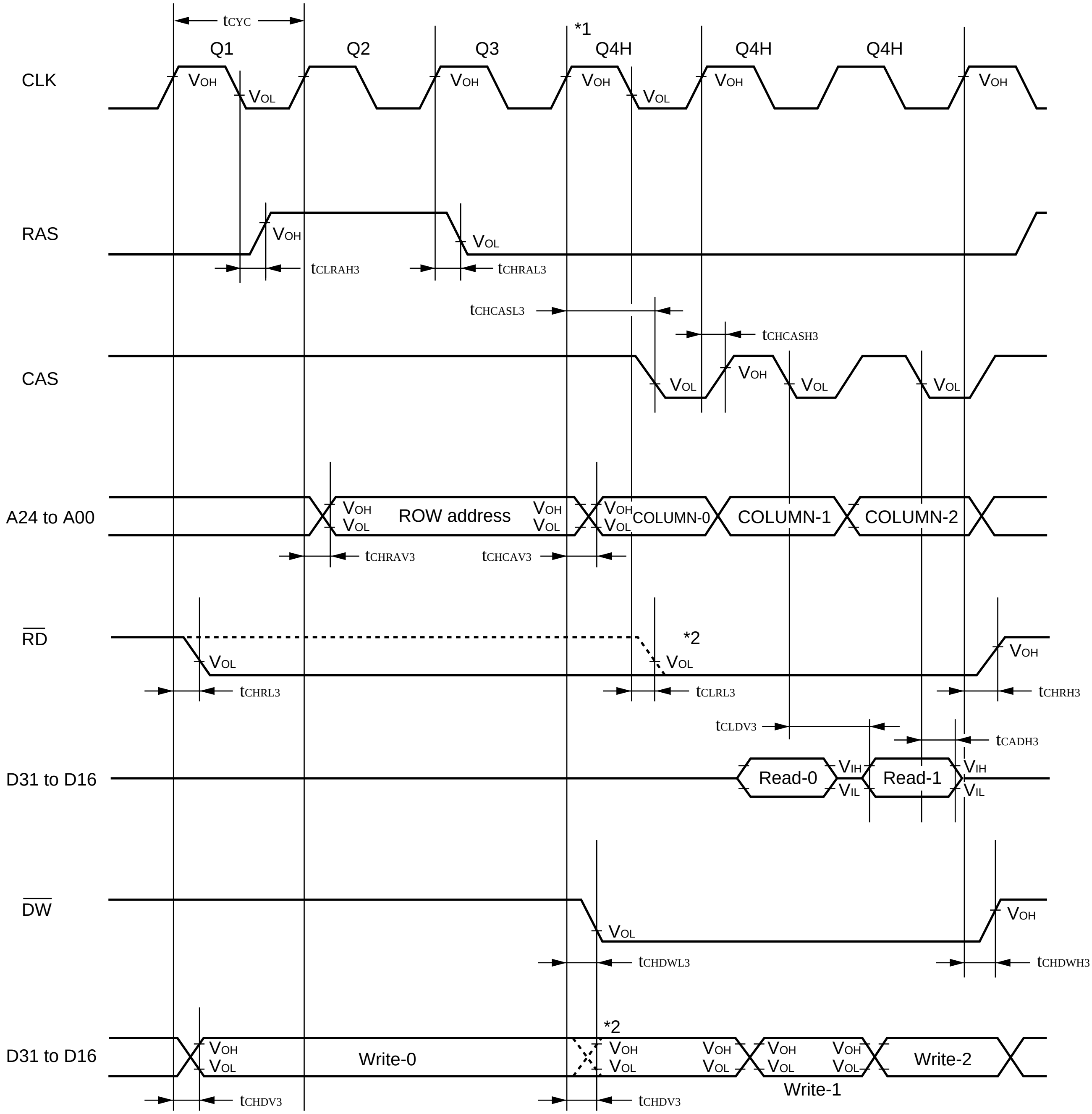


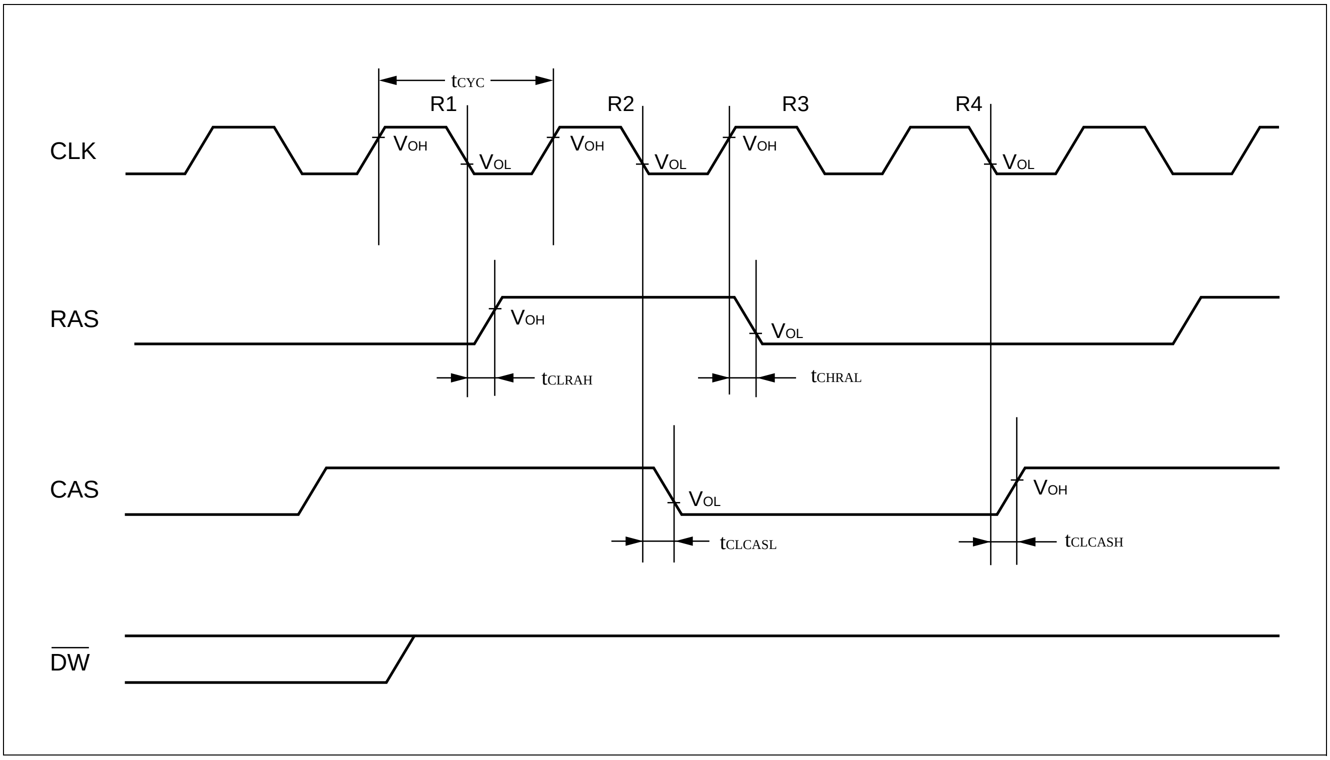
*1: Q4S indicates Q4SR (Read) of Single DRAM cycle or Q4SW (Write) cycle.
*2: - - - - indicates the timing when the bus cycle begins from the high spead page mode.

(13) CBR Refresh

($V_{CC}5$ = 5.0 V ±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = 0°C to +70°C)
($V_{CC}5$ = $V_{CC}3$ = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, T_A = 0°C to +70°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
RAS delay time	t_{CLRAH}	CLK, RAS	—	—	6	ns	
	t_{CHRAL}	CLK, RAS		—	6	ns	
CAS delay time	t_{CLCASL}	CLK, CAS		—	6	ns	
	t_{CLCASH}	CLK, CAS		—	6	ns	

CAS: CS0L to CS1H pins are for CAS signal outputs.



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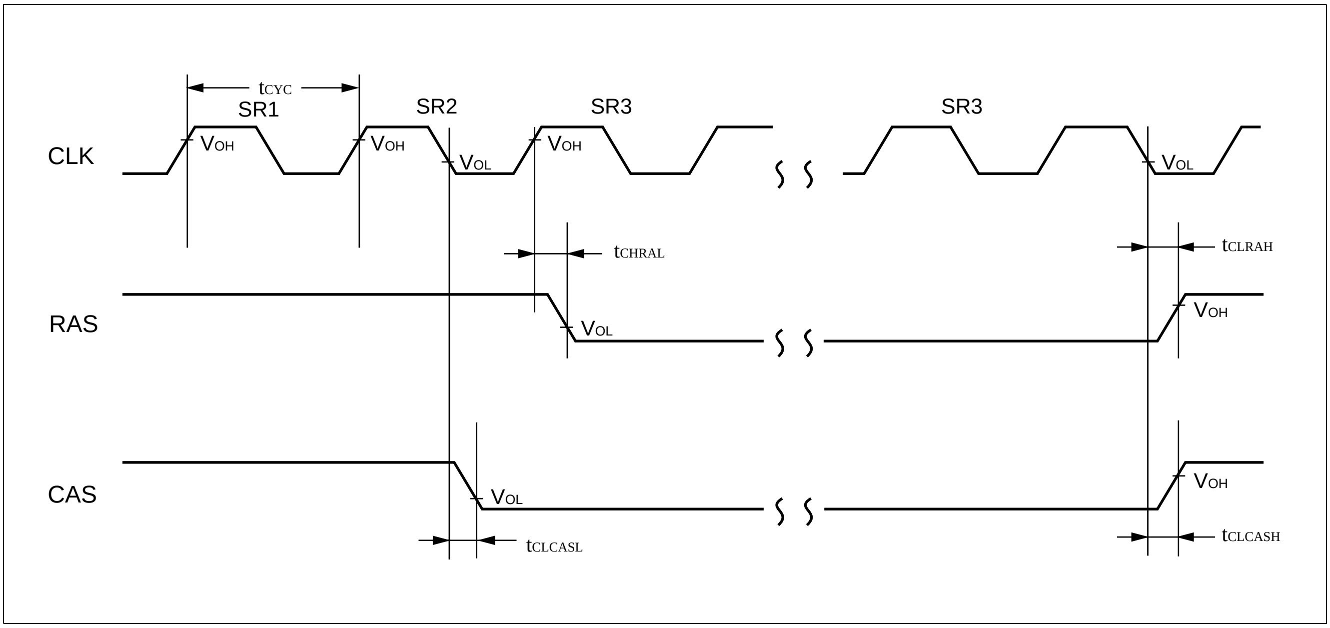
(14) Self Refresh

($V_{CC}5$ = 5.0 V ±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = 0°C to +70°C)
($V_{CC}5$ = $V_{CC}3$ = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, T_A = 0°C to +70°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
RAS delay time	t_{CLRAH}	CLK, RAS	—	—	6	ns	
	t_{CHRAL}	CLK, RAS		—	6	ns	
CAS delay time	t_{CLCASL}	CLK, CAS		—	6	ns	
	t_{CLCASH}	CLK, CAS		—	6	ns	

CAS: CS0L to CS1H pins are for CAS signal outputs.



(15) UART Timing

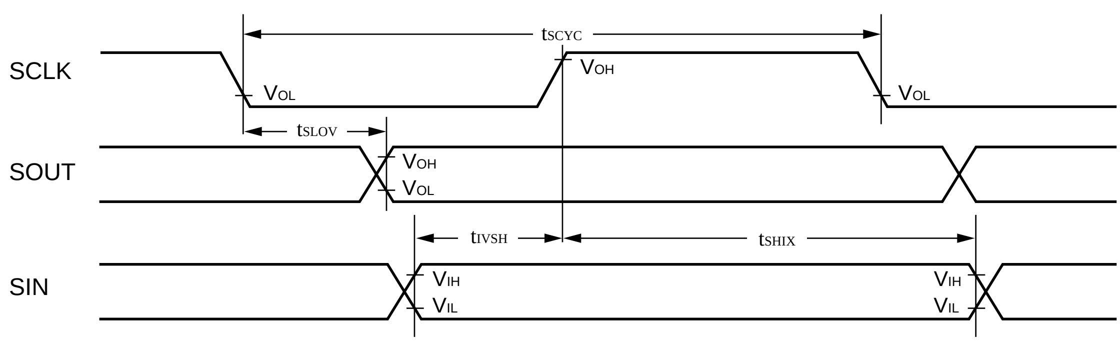
($V_{CC}5$ = 5.0 V ±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = 0°C to +70°C)
($V_{CC}5$ = $V_{CC}3$ = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, T_A = 0°C to +70°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Serial clock cycle time	t_{SCYC}	—	Internal shift clock mode	8 × t_{CYCP}	—	ns	
SCLK ↓→ SOUT delay time	t_{SLOV}	—		–80	80	ns	
Valid SIN → SCLK ↑	t_{IVSH}	—		100	—	ns	
SCLK ↑→ valid SIN hold time	t_{SHIX}	—		60	—	ns	
Serial clock “H” pulse width	t_{SHSL}	—	External shift clock mode	4 × t_{CYCP}	—	ns	
Serial clock “L” pulse width	t_{SLSH}	—		4 × t_{CYCP}	—	ns	
SCLK ↓→ SOUT delay time	t_{SLOV}	—		—	150	ns	
Valid SIN → SCLK ↑	t_{IVSH}	—		60	—	ns	
SCLK ↑→ valid SIN hold time	t_{SHIX}	—		60	—	ns	

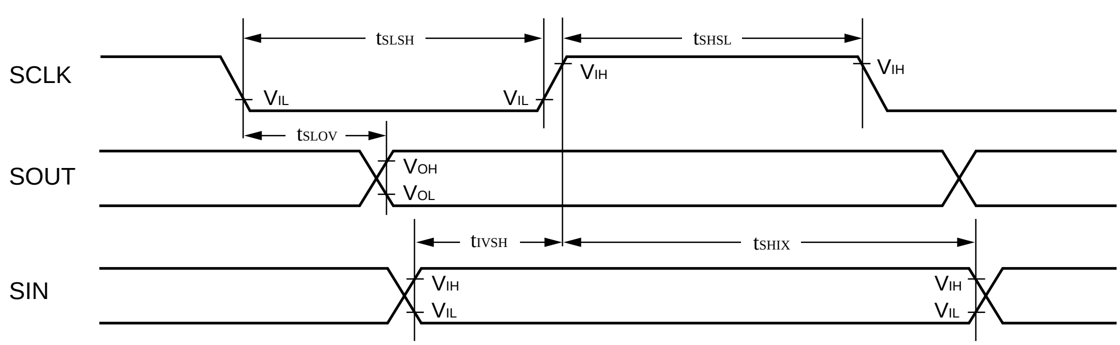
t_{CYCP}: A cycle time of peripheral system clock

Notes: This rating is for AC characteristics in CLK synchronous mode.

- **Internal shift clock mode**



- **External shift clock mode**



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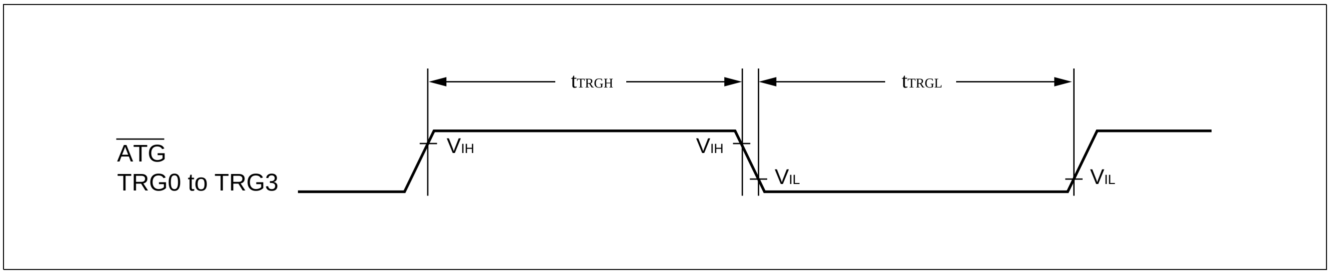
(16) Trigger System Input Timing

($V_{CC}5$ = 5.0 V ±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = 0°C to +70°C)
($V_{CC}5$ = $V_{CC}3$ = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, T_A = 0°C to +70°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
A/D start trigger input time	t_{TRGH}, t_{TRGL}	$\overline{ATG}$	—	5 × t_{CYCP}	—	ns	
PWM external trigger input time	t_{TRGH}, t_{TRGL}	TRG0 to TRG3		5 × t_{CYCP}	—	ns	
External interrupt input time	t_{INT}	INT0 to INT3		5 × t_{CYCP}	—	ns	

t_{CYCP}: A cycle time of peripheral system clock

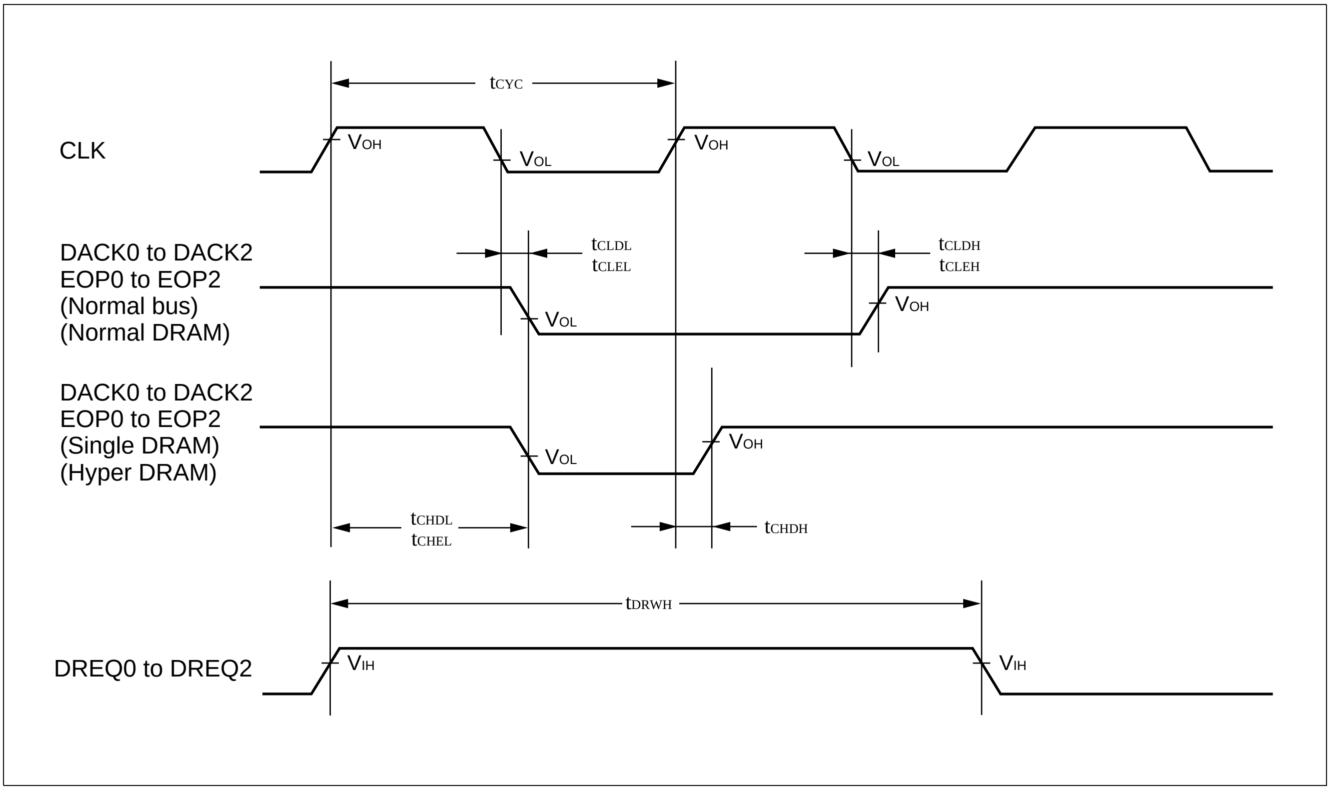


(17) DMA Controller Timing

($V_{CC}5$ = 5.0 V ±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = 0°C to +70°C)
($V_{CC}5$ = $V_{CC}3$ = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, T_A = 0°C to +70°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
DREQ input pulse width	t_{DRWH}	DREQ0 to DREQ2	—	2 × t_{CYC}	—	ns	
DACK delay time (Normal bus) (Normal DRAM)	t_{CLDL}	CLK, DACK0 to DACK2		—	6	ns	
	t_{CLDH}	CLK, DACK0 to DACK2		—	6	ns	
EOP delay time (Normal bus) (Normal DRAM)	t_{CLEL}	CLK, EOP0 to EOP2		—	6	ns	
	t_{CLEH}	CLK, EOP0 to EOP2		—	6	ns	
DACK delay time (Single DRAM) (Hyper DRAM)	t_{CHDL}	CLK, DACK0 to DACK2		—	n/2 × t_{CYC}	ns	
	t_{CHDH}	CLK, DACK0 to DACK2		—	6	ns	
EOP delay time (Single DRAM) (Hyper DRAM)	t_{CHEL}	CLK, EOP0 to EOP2		—	n/2 × t_{CYC}	ns	
	t_{CHEH}	CLK, EOP0 to EOP2		—	6	ns	

t_{CYC} (a cycle time of peripheral system clock): Refer to “(3) Clock Output Timing.”



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5. A/D Converter Block Electrical Characteristics

(AV_{CC} = 2.7 V to 3.6 V, AV_{SS} = 0.0 V, AVRH = 2.7 V, T_A = 0°C to +70°C)

Parameter	Symbol	Pin name	Value			Unit
			Min.	Typ.	Max.	
Resolution	—	—	—	10	10	bit
Total error	—	—	—	—	±4.0	LSB
Linearity error	—	—	—	—	±3.5	LSB
Differentiation linearity error	—	—	—	—	±2.0	LSB
Zero transition voltage	V_{OT}	AN0 to AN3	–1.5	+0.5	+2.5	LSB
Full-scale transition voltage	V_{FST}	AN0 to AN3	AVRH – 4.5	AVRH – 1.5	AVRH + 0.5	LSB
Conversion time	—	—	5.6 *1	—	—	µs
Analog port input current	I_{AIN}	AN0 to AN3	—	0.1	10	µA
Analog input voltage	V_{AIN}	AN0 to AN3	AV_{SS}	—	AVRH	V
Reference voltage	—	AVRH	AV_{SS}	—	AV_{CC}	V
Power supply current	I_A	AV_{CC}	—	4	—	mA
	I_{AH}	AV_{CC}	—	—	5 *2	µA
Reference voltage supply current	I_R	AVRH	—	200	—	µA
	I_{RH}	AVRH	—	—	5 *2	µA
Conversion variance between channels	—	AN0 to AN3	—	—	4	LSB

*1: AV_{CC} = 2.7 V – 3.6 V

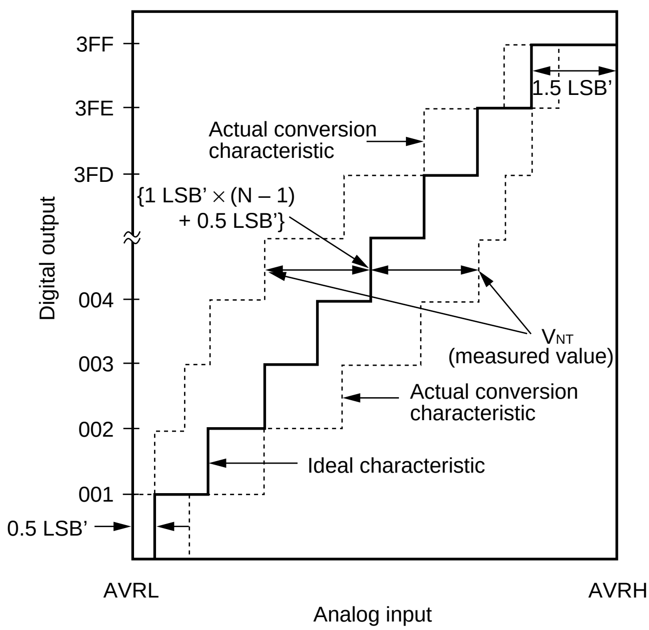
*2: Current value for A/D converters not in operation, CPU stop mode (V_{CC} = AV_{CC} = AVRH = 3.6 V)

Notes:
- As the absolute value of AVRH decreases, relative error increases.
- Output impedance of external circuit of analog input under following conditions;
  Output impedance of external circuit < 10 kΩ.
  If output impedance of external circuit is too high, analog voltage sampling time may be too short for accurate sampling (sampling time is 5.6 µs for a machine clock of 25 MHz).

6. A/D Converter Glossary

- Resolution
  The smallest change in analog voltage detected by A/D converter.
- Linearity error
  A deviation of actual conversion characteristic from a line connecting the zero-traction point (between "00 0000 0000" ↔ "00 0000 0001") to the full-scale transition point (between "11 1111 1110" ↔ "11 1111 1111").
- Differential linearity error
  A deviation of a step voltage for changing the LSB of output code from ideal input voltage.
- Total error
  A difference between actual value and theoretical value. The overall error includes zero-transition error, full-scale transition error and linearity error.

Total error



$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ LSB' \times (N - 1) + 0.5\ LSB'\}}{1\ LSB'}\ [LSB]$$

V_{OT}' (ideal value) = AVRL + 0.5 LSB' [V]

V_{FST}' (ideal value) = AVRL + 1.5 LSB' [V]

V_{NT}: A voltage for causing transition of digital output from (N – 1) to N

(Continued)

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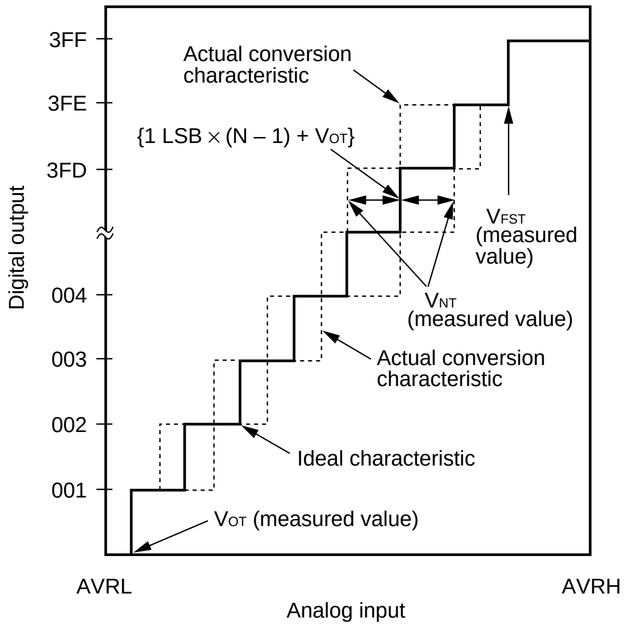
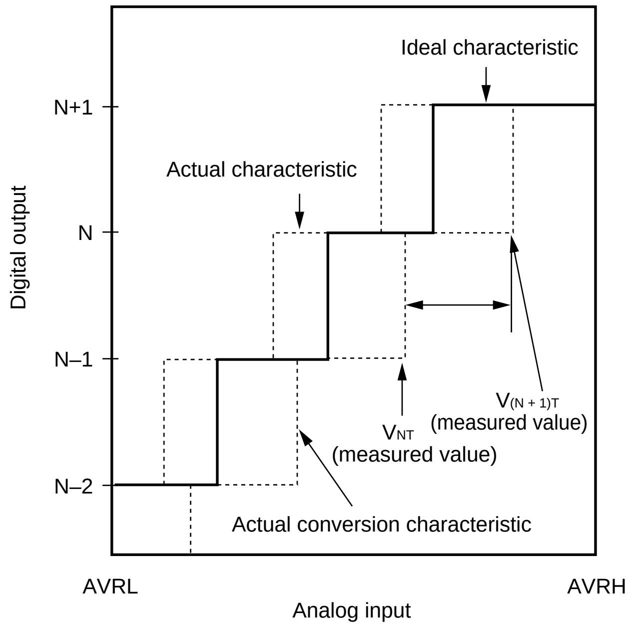
(Continued)

Linearity error



Differential linearity error



$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1\ LSB' \times (N - 1) + V_{OT}\}}{1\ LSB}\ [LSB]$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ LSB} - 1\ [LSB]$$

$$1\ LSB = \frac{V_{FST} - V_{OT}}{1022}\ [V]$$

$$1\ LSB'\ (\text{ideal value}) = \frac{AVRH - AVRL}{1024}\ [V]$$

V_{OT}: A voltage for causing transition of digital output from $(000)_H$ to $(001)_H$

V_{FST}: A voltage for causing transition of digital output from $(3FE)_H$ to $(3FF)_H$

V_{NT}: A voltage for causing transition of digital output from $(N - 1)_H$ to N

■ INSTRUCTIONS (165 INSTRUCTIONS)

1. How to Read Instruction Set Summary

Mnemonic	Type	OP	CYC	NZVC	Operation	Remarks
ADD Rj, Ri	A	A6	1	CCCC	Ri + Rj → Ri	
* ADD #s5, Ri	C	A4	1	CCCC	Ri + s5 → Ri	
,	,	,	,	,	,	
,	,	,	,	,	,	
↓ (1) ↓ (2)	↓ (3)	↓ (4)	↓ (5)	↓ (6)	↓ (7)	

(1) Names of instructions
Instructions marked with * are not included in CPU specifications. These are extended instruction codes added/extended at assembly language levels.

(2) Addressing modes specified as operands are listed in symbols.
Refer to “2. Addressing mode symbols” for further information.

(3) Instruction types

(4) Hexa-decimal expressions of instructions

(5) The number of machine cycles needed for execution

a: Memory access cycle and it has possibility of delay by Ready function.

b: Memory access cycle and it has possibility of delay by Ready function.
If an object register in a LD operation is referenced by an immediately following instruction, the interlock function is activated and number of cycles needed for execution increases.

c: If an immediately following instruction operates to an object of R15, SSP or USP in read/write mode or if the instruction belongs to instruction format A group, the interlock function is activated and number of cycles needed for execution increases by 1 to make the total number of 2 cycles needed.

d: If an immediately following instruction refers to MDH/MDL, the interlock function is activated and number of cycles needed for execution increases by 1 to make the total number of 2 cycles needed.

For a, b, c and d, minimum execution cycle is 1.

(6) Change in flag sign

- Flag change
  C : Change
  – : No change
  0 : Clear
  1 : Set
- Flag meanings
  N : Negative flag
  Z : Zero flag
  V : Over flag
  C : Carry flag

(7) Operation carried out by instruction

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2. Addressing Mode Symbols

Ri	: Register direct (R0 to R15, AC, FP, SP)
Rj	: Register direct (R0 to R15, AC, FP, SP)
R13	: Register direct (R13, AC)
Ps	: Register direct (Program status register)
Rs	: Register direct (TBR, RP, SSP, USP, MDH, MDL)
CRi	: Register direct (CR0 to CR15)
CRj	: Register direct (CR0 to CR15)
#i8	: Unsigned 8-bit immediate (–128 to 255) Note: –128 to –1 are interpreted as 128 to 255
#i20	: Unsigned 20-bit immediate (–0X80000 to 0XFFFFF) Note: –0X7FFFF to –1 are interpreted as 0X7FFFF to 0XFFFFF
#i32	: Unsigned 32-bit immediate (–0X80000000 to 0XFFFFFFFF) Note: –0X80000000 to –1 are interpreted as 0X80000000 to 0XFFFFFFFF
#s5	: Signed 5-bit immediate (–16 to 15)
#s10	: Signed 10-bit immediate (–512 to 508, multiple of 4 only)
#u4	: Unsigned 4-bit immediate (0 to 15)
#u5	: Unsigned 5-bit immediate (0 to 31)
#u8	: Unsigned 8-bit immediate (0 to 255)
#u10	: Unsigned 10-bit immediate (0 to 1020, multiple of 4 only)
@dir8	: Unsigned 8-bit direct address (0 to 0XFF)
@dir9	: Unsigned 9-bit direct address (0 to 0X1FE, multiple of 2 only)
@dir10	: Unsigned 10-bit direct address (0 to 0X3FC, multiple of 4 only)
label9	: Signed 9-bit branch address (–0X100 to 0XFC, multiple of 2 only)
label12	: Signed 12-bit branch address (–0X800 to 0X7FC, multiple of 2 only)
label20	: Signed 20-bit branch address (–0X80000 to 0X7FFFF)
label32	: Signed 32-bit branch address (–0X80000000 to 0X7FFFFFFF)
@Ri	: Register indirect (R0 to R15, AC, FP, SP)
@Rj	: Register indirect (R0 to R15, AC, FP, SP)
@(R13, Rj)	: Register relative indirect (Rj: R0 to R15, AC, FP, SP)
@(R14, disp10)	: Register relative indirect (disp10: –0X200 to 0X1FC, multiple of 4 only)
@(R14, disp9)	: Register relative indirect (disp9: –0X100 to 0XFE, multiple of 2 only)
@(R14, disp8)	: Register relative indirect (disp8: –0X80 to 0X7F)
@(R15, udisp6)	: Register relative (udisp6: 0 to 60, multiple of 4 only)
@Ri+	: Register indirect with post-increment (R0 to R15, AC, FP, SP)
@R13+	: Register indirect with post-increment (R13, AC)
@SP+	: Stack pop
@–SP	: Stack push
(reglist)	: Register list

3. Instruction Types

MSB — 16 bits — LSB

Type A

OP	Rj	Ri
8	4	4

Type B

OP	i8/o8	Ri
4	8	4

Type C

OP	u4/m4	Ri
8	4	4

Type *C’

ADD, ADDN, CMP, LSL, LSR and ASR instructions only

OP	s5/u5	Ri
7	5	4

Type D

OP	u8/rel8/dir/reglist
8	8

Type E

OP	SUB-OP	Ri
8	4	4

Type F

OP	rel11
5	11

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4. Detailed Description of Instructions

- **Add/subtract operation instructions (10 instructions)**

Mnemonic		Type	OP	Cycle	N Z V C	Operation	Remarks
ADD	Rj, Ri	A	A6	1	C C C C	Ri + Rj → Ri	
* ADD	#s5, Ri	C'	A4	1	C C C C	Ri + s5 → Ri	MSB is interpreted as a sign in assembly language
ADD	#i4, Ri	C	A4	1	C C C C	Ri + extu (i4) → Ri	Zero-extension
ADD2	#i4, Ri	C	A5	1	C C C C	Ri + extu (i4) → Ri	Sign-extension
ADDC	Rj, Ri	A	A7	1	C C C C	Ri + Rj + c → Ri	Add operation with sign
ADDN	Rj, Ri	A	A2	1	– – – –	Ri + Rj → Ri	
* ADDN	#s5, Ri	C'	A0	1	– – – –	Ri + s5 → Ri	MSB is interpreted as a sign in assembly language
ADDN	#i4, Ri	C	A0	1	– – – –	Ri + extu (i4) → Ri	Zero-extension
ADDN2	#i4, Ri	C	A1	1	– – – –	Ri + extu (i4) → Ri	Sign-extension
SUB	Rj, Ri	A	AC	1	C C C C	Ri – Rj → Ri	
SUBC	Rj, Ri	A	AD	1	C C C C	Ri – Rj – c → Ri	Subtract operation with carry
SUBN	Rj, Ri	A	AE	1	– – – –	Ri – Rj → Ri	

- **Compare operation instructions (3 instructions)**

Mnemonic		Type	OP	Cycle	N Z V C	Operation	Remarks
CMP	Rj, Ri	A	AA	1	C C C C	Ri – Rj	
* CMP	#s5, Ri	C'	A8	1	C C C C	Ri – s5	MSB is interpreted as a sign in assembly language
CMP	#i4, Ri	C	A8	1	C C C C	Ri + extu (i4)	Zero-extension
CMP2	#i4, Ri	C	A9	1	C C C C	Ri + extu (i4)	Sign-extension

- **Logical operation instructions (12 instructions)**

Mnemonic		Type	OP	Cycle	N Z V C	Operation	Remarks
AND	Rj, Ri	A	82	1	C C – –	Ri & = Rj	Word
AND	Rj, @Ri	A	84	1 + 2a	C C – –	(Ri) & = Rj	Word
ANDH	Rj, @Ri	A	85	1 + 2a	C C – –	(Ri) & = Rj	Half word
ANDB	Rj, @Ri	A	86	1 + 2a	C C – –	(Ri) & = Rj	Byte
OR	Rj, Ri	A	92	1	C C – –	Ri | = Rj	Word
OR	Rj, @Ri	A	94	1 + 2a	C C – –	(Ri) | = Rj	Word
ORH	Rj, @Ri	A	95	1 + 2a	C C – –	(Ri) | = Rj	Half word
ORB	Rj, @Ri	A	96	1 + 2a	C C – –	(Ri) | = Rj	Byte
EOR	Rj, Ri	A	9A	1	C C – –	Ri ^ = Rj	Word
EOR	Rj, @Ri	A	9C	1 + 2a	C C – –	(Ri) ^ = Rj	Word
EORH	Rj, @Ri	A	9D	1 + 2a	C C – –	(Ri) ^ = Rj	Half word
EORB	Rj, @Ri	A	9E	1 + 2a	C C – –	(Ri) ^ = Rj	Byte

• **Bit manipulation arithmetic instructions (8 instructions)**

Mnemonic		Type	OP	Cycle	N Z V C	Operation	Remarks
BANDL	#u4, @Ri (u4: 0 to 0FH)	C	80	1 + 2a	– – – –	(Ri) & = (F0H + u4)	Manipulate lower 4 bits
BANDH	#u4, @Ri (u4: 0 to 0FH)	C	81	1 + 2a	– – – –	(Ri) & = ((u4<<4) + 0FH)	Manipulate upper 4 bits
* BAND	#u8, @Ri *1			–	– – – –	(Ri) & = u8	
BORL	#u4, @Ri (u4: 0 to 0FH)	C	90	1 + 2a	– – – –	(Ri) | = u4	Manipulate lower 4 bits
BORH	#u4, @Ri (u4: 0 to 0FH)	C	91	1 + 2a	– – – –	(Ri) | = (u4<<4)	Manipulate upper 4 bits
* BOR	#u8, @Ri *2			–	– – – –	(Ri) | = u8	
BEORL	#u4, @Ri (u4: 0 to 0FH)	C	98	1 + 2a	– – – –	(Ri) ^ = u4	Manipulate lower 4 bits
BEORH	#u4, @Ri (u4: 0 to 0FH)	C	99	1 + 2a	– – – –	(Ri) ^ = (u4<<4)	Manipulate upper 4 bits
* BEOR	#u8, @Ri *3			–	– – – –	(Ri) ^ = u8	
BTSTL	#u4, @Ri (u4: 0 to 0FH)	C	88	2 + a	0 C – –	(Ri) & u4	Test lower 4 bits
BTSTH	#u4, @Ri (u4: 0 to 0FH)	C	89	2 + a	C C – –	(Ri) & (u4<<4)	Test upper 4 bits

*1: Assembler generates BANDL if result of logical operation “u8&0x0F” leaves an active (set) bit and generates BANDH if “u8&0xF0” leaves an active bit. Depending on the value in the “u8” format, both BANDL and BANDH may be generated.
*2: Assembler generates BORL if result of logical operation “u8&0x0F” leaves an active (set) bit and generates BORH if “u8&0xF0” leaves an active bit.
*3: Assembler generates BEORL if result of logical operation “u8&0x0F” leaves an active (set) bit and generates BEORH if “u8&0xF0” leaves an active bit.

• **Add/subtract operation instructions (10 instructions)**

Mnemonic		Type	OP	Cycle	N Z V C	Operation	Remarks
MUL	Rj, Ri	A	AF	5	C C C –	Rj × Ri → MDH, MDL	32-bit × 32-bit = 64-bit
MULU	Rj, Ri	A	AB	5	C C C –	Rj × Ri → MDH, MDL	Unsigned
MULH	Rj, Ri	A	BF	3	C C – –	Rj × Ri → MDL	16-bit × 16-bit = 32-bit
MULUH	Rj, Ri	A	BB	3	C C – –	Rj × Ri → MDL	Unsigned
DIVOS	Ri	E	97 – 4	1	– – – –		Step calculation
DIVOU	Ri	E	97 – 5	1	– – – –		32-bit/32-bit = 32-bit
DIV1	Ri	E	97 – 6	d	– C – C		
DIV2	Ri	E	97 – 7	1	– C – C		
DIV3		E	9F – 6	1	– – – –		
DIV4S		E	9F – 7	1	– – – –		
* DIV	Ri *1			–	– C – C	MDL/Ri → MDL, MDL%Ri → MDH	
* DIVU	Ri *2			–	– C – C	MDL/Ri → MDL, MDL%Ri → MDH	Unsigned

*1: DIVOS, DIV1 × 32, DIV2, DIV3 and DIV4S are generated. A total instruction code length of 72 bytes.
*2: DIVOU and DIV1 × 32 are generated. A total instruction code length of 66 bytes.

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- **Shift arithmetic instructions (9 instructions)**

Mnemonic		Type	OP	Cycle	N Z V C	Operation	Remarks
LSL	Rj, Ri	A	B6	1	C C – C	Ri<<Rj → Ri	Logical shift
* LSL	#u5, Ri	C'	B4	1	C C – C	Ri<<u5 → Ri	
LSL	#u4, Ri	C	B4	1	C C – C	Ri<<u4 → Ri	
LSL2	#u4, Ri	C	B5	1	C C – C	Ri<<(u4 + 16) → Ri	
LSR	Rj, Ri	A	B2	1	C C – C	Ri>>Rj → Ri	Logical shift
* LSR	#u5, Ri	C'	B0	1	C C – C	Ri>>u5 → Ri	
LSR	#u4, Ri	C	B0	1	C C – C	Ri>>u4 → Ri	
LSR2	#u4, Ri	C	B1	1	C C – C	Ri>>(u4 + 16) → Ri	
ASR	Rj, Ri	A	BA	1	C C – C	Ri>>Rj → Ri	Logical shift
* ASR	#u5, Ri	C'	B8	1	C C – C	Ri>>u5 → Ri	
ASR	#u4, Ri	C	B8	1	C C – C	Ri>>u4 → Ri	
ASR2	#u4, Ri	C	B9	1	C C – C	Ri>>(u4 + 16) → Ri	

- **Immediate value data transfer instruction (immediate value set/16-bit/32-bit immediate value transfer instruction) (3 instructions)**

Mnemonic		Type	OP	Cycle	N Z V C	Operation	Remarks
LDI: 32	#i32, Ri	E	9F – 8	3	– – – –	i32 → Ri	
LDI: 20	#i20, Ri	C	9B	2	– – – –	i20 → Ri	Upper 12 bits are zero-extended
LDI: 8	#i8, Ri	B	C0	1	– – – –	i8 → Ri	Upper 24 bits are zero-extended
* LDI	# {i8 | i20 | i32}, Ri *1					{i8 | i20 | i32} → Ri	

*1: If an immediate value is given in absolute, assembler automatically makes i8, i20 or i32 selection.
If an immediate value contains relative value or external reference, assembler selects i32.

- **Memory load instructions (13 instructions)**

Mnemonic		Type	OP	Cycle	N Z V C	Operation	Remarks
LD	@Rj, Ri	A	04	b	– – – –	(Rj) → Ri	
LD	@(R13, Rj), Ri	A	00	b	– – – –	(R13 + Rj) → Ri	
LD	@(R14, disp10), Ri	B	20	b	– – – –	(R14 + disp10) → Ri	
LD	@(R15, udisp6), Ri	C	03	b	– – – –	(R15 + udisp6) → Ri	
LD	@R15 +, Ri	E	07 – 0	b	– – – –	(R15) → Ri, R15 + = 4	
LD	@R15 +, Rs	E	07 – 8	b	– – – –	(R15) → Rs, R15 + = 4	Rs: Special-purpose register
LD	@R15 +, PS	E	07 – 9	1 + a + b	C C C C	(R15) → PS, R15 + = 4	
LDUH	@Rj, Ri	A	05	b	– – – –	(Rj) → Ri	Zero-extension
LDUH	@(R13, Rj), Ri	A	01	b	– – – –	(R13 + Rj) → Ri	Zero-extension
LDUH	@(R14, disp9), Ri	B	40	b	– – – –	(R14 + disp9) → Ri	Zero-extension
LDUB	@Rj, Ri	A	06	b	– – – –	(Rj) → Ri	Zero-extension
LDUB	@(R13, Rj), Ri	A	02	b	– – – –	(R13 + Rj) → Ri	Zero-extension
LDUB	@(R14, disp8), Ri	B	60	b	– – – –	(R14 + disp8) → Ri	Zero-extension

Note: The relations between o8 field of TYPE-B and u4 field of TYPE-C in the instruction format and assembler description from disp8 to disp10 are as follows:

disp8 → o8 = disp8
disp9 → o8 = disp9>>1
disp10 → o8 = disp10>>2
} Each disp is a code extension.

udisp6 → u4 = udisp6>>2 udisp4 is a 0 extension.

- **Memory store instructions (13 instructions)**

Mnemonic		Type	OP	Cycle	N Z V C	Operation	Remarks
ST	Ri, @Rj	A	14	a	– – – –	Ri → (Rj)	Word
ST	Ri, @(R13, Rj)	A	10	a	– – – –	Ri → (R13 + Rj)	Word
ST	Ri, @(R14, disp10)	B	30	a	– – – –	Ri → (R14 + disp10)	Word
ST	Ri, @(R15, udisp6)	C	13	a	– – – –	Ri → (R15 + usidp6)	
ST	Ri, @–R15	E	17 – 0	a	– – – –	R15 – = 4, Ri → (R15)	
ST	Rs, @–R15	E	17 – 8	a	– – – –	R15 – = 4, Rs → (R15)	Rs: Special-purpose register
ST	PS, @–R15	E	17 – 9	a	– – – –	R15 – = 4, PS → (R15)	
STH	Ri, @Rj	A	15	a	– – – –	Ri → (Rj)	Half word
STH	Ri, @(R13, Rj)	A	11	a	– – – –	Ri → (R13 + Rj)	Half word
STH	Ri, @(R14, disp9)	B	50	a	– – – –	Ri → (R14 + disp9)	Half word
STB	Ri, @Rj	A	16	a	– – – –	Ri → (Rj)	Byte
STB	Ri, @(R13, Rj)	A	12	a	– – – –	Ri → (R13 + Rj)	Byte
STB	Ri, @(R14, disp8)	B	70	a	– – – –	Ri → (R14 + disp8)	Byte

Note: The relations between o8 field of TYPE-B and u4 field of TYPE-C in the instruction format and assembler description from disp8 to disp10 are as follows:

disp8 → o8 = disp8
disp9 → o8 = disp9>>1
disp10 → o8 = disp10>>2
} Each disp is a code extension.
udisp6 → u4 = udisp6>>2 udisp4 is a 0 extension.

- **Transfer instructions between registers/special-purpose registers transfer instructions (5 instructions)**

Mnemonic		Type	OP	Cycle	N Z V C	Operation	Remarks
MOV	Rj, Ri	A	8B	1	– – – –	Rj → Ri	Transfer between general-purpose registers
MOV	Rs, Ri	A	B7	1	– – – –	Rs → Ri	Rs: Special-purpose register
MOV	Ri, Rs	A	B3	1	– – – –	Ri → Rs	Rs: Special-purpose register
MOV	PS, Ri	E	17 – 1	1	– – – –	PS → Ri	
MOV	Ri, PS	E	07 – 1	c	C C C C	Ri → PS	

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- **Non-delay normal branch instructions (23 instructions)**

Mnemonic		Type	OP	Cycle	N Z V C	Operation	Remarks
JMP	@Ri	E	97 – 0	2	– – – –	Ri → PC	
CALL	label12	F	D0	2	– – – –	PC + 2 → RP, PC + 2 + rel11 × 2 → PC	
CALL	@Ri	E	97 – 1	2	– – – –	PC + 2 → RP, Ri → PC	
RET		E	97 – 2	2	– – – –	RP → PC	Return
INT	#u8	D	1F	3+3a	– – – –	SSP – = 4, PS → (SSP), SSP – = 4, PC + 2 → (SSP), 0 → I flag, 0 → S flag, (TBR + 3FC – u8 × 4) → PC	
INTE		E	9F – 3	3 + 3a	– – – –	SSP – = 4, PS → (SSP), SSP – = 4, PC + 2 → (SSP), 0 → S flag, (TBR + 3D8 – u8 × 4) → PC	For emulator
RETI		E	97 – 3	2 + 2a	C C C C	(R15) → PC, R15 – = 4, (R15) → PS, R15 – = 4	
BNO	label9	D	E1	1	– – – –	Non-branch	
BRA	label9	D	E0	2	– – – –	PC + 2 + rel8 × 2 → PC	
BEQ	label9	D	E2	2/1	– – – –	PCif Z = = 1	
BNE	label9	D	E3	2/1	– – – –	PCif Z = = 0	
BC	label9	D	E4	2/1	– – – –	PCif C = = 1	
BNC	label9	D	E5	2/1	– – – –	PCif C = = 0	
BN	label9	D	E6	2/1	– – – –	PCif N = = 1	
BP	label9	D	E7	2/1	– – – –	PCif N = = 0	
BV	label9	D	E8	2/1	– – – –	PCif V = = 1	
BNV	label9	D	E9	2/1	– – – –	PCif V = = 0	
BLT	label9	D	EA	2/1	– – – –	PCif V xor N = = 1	
BGE	label9	D	EB	2/1	– – – –	PCif V xor N = = 0	
BLE	label9	D	EC	2/1	– – – –	PCif (V xor N) or Z = = 1	
BGT	label9	D	ED	2/1	– – – –	PCif (V xor N) or Z = = 0	
BLS	label9	D	EE	2/1	– – – –	PCif C or Z = = 1	
BHI	label9	D	EF	2/1	– – – –	PCif C or Z = = 0	

Notes:
- "2/1" in cycle sections indicates that 2 cycles are needed for branch and 1 cycle needed for non-branch.
- The relations between rel8 field of TYPE-D and rel11 field of TYPE-F in the instruction format and assembler discription label9 and label12 are as follows.
  label9 → rel8 = (label9 – PC – 2)/2
  label12 → rel11 = (label12 – PC – 2)/2
- RETI must be operated while S flag = 0.

- **Branch instructions with delays (20 instructions)**

Mnemonic		Type	OP	Cycle	N Z V C	Operation	Remarks
JMP:D	@Ri	E	9F – 0	1	– – – –	Ri → PC	
CALL:D	label12	F	D8	1	– – – –	PC + 4 → RP, PC + 2 + rel11 × 2 → PC	
CALL:D	@Ri	E	9F – 1	1	– – – –	PC + 4 → RP, Ri → PC	
RET:D		E	9F – 2	1	– – – –	RP → PC	Return
BNO:D	label9	D	F1	1	– – – –	Non-branch	
BRA:D	label9	D	F0	1	– – – –	PC + 2 + rel8 × 2 → PC	
BEQ:D	label9	D	F2	1	– – – –	PCif Z = = 1	
BNE:D	label9	D	F3	1	– – – –	PCif Z = = 0	
BC:D	label9	D	F4	1	– – – –	PCif C = = 1	
BNC:D	label9	D	F5	1	– – – –	PCif C = = 0	
BN:D	label9	D	F6	1	– – – –	PCif N = = 1	
BP:D	label9	D	F7	1	– – – –	PCif N = = 0	
BV:D	label9	D	F8	1	– – – –	PCif V = = 1	
BNV:D	label9	D	F9	1	– – – –	PCif V = = 0	
BLT:D	label9	D	FA	1	– – – –	PCif V xor N = = 1	
BGE:D	label9	D	FB	1	– – – –	PCif V xor N = = 0	
BLE:D	label9	D	FC	1	– – – –	PCif (V xor N) or Z = = 1	
BGT:D	label9	D	FD	1	– – – –	PCif (V xor N) or Z = = 0	
BLS:D	label9	D	FE	1	– – – –	PCif C or Z = = 1	
BHI:D	label9	D	FF	1	– – – –	PCif C or Z = = 0	

Notes:
- The relations between rel8 field of TYPE-D and rel11 field of TYPE-F in the instruction format and assembler discription label9 and label12 are as follows.
  label9 → rel8 = (label9 – PC – 2)/2
  label12 → rel11 = (label12 – PC – 2)/2
- Delayed branch operation always executes next instruction (delay slot) before making a branch.
- Instructions allowed to be stored in the delay slot must meet one of the following conditions. If the other instruction is stored, this device may operate other operation than defined.
  The instruction described “1” in the other cycle column than branch instruction.
  The instruction described “a”, “b”, “c” or “d” in the cycle column.

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- **Direct addressing instructions**

Mnemonic	Type	OP	Cycle	N Z V C	Operation	Remarks
DMOV @dir10, R13	D	08	b	– – – –	(dir10) → R13	Word
DMOV R13, @dir10	D	18	a	– – – –	R13 → (dir10)	Word
DMOV @dir10, @R13+	D	0C	2a	– – – –	(dir10) → (R13), R13 + = 4	Word
DMOV @R13+, @dir10	D	1C	2a	– – – –	(R13) → (dir10), R13 + = 4	Word
DMOV @dir10, @–R15	D	0B	2a	– – – –	R15 – = 4, (dir10) → (R15)	Word
DMOV @R15+, @dir10	D	1B	2a	– – – –	(R15) → (dir10), R15 + = 4	Word
DMOVH @dir9, R13	D	09	b	– – – –	(dir9) → R13	Half word
DMOVH R13, @dir9	D	19	a	– – – –	R13 → (dir9)	Half word
DMOVH @dir9, @R13+	D	0D	2a	– – – –	(dir9) → (R13), R13 + = 2	Half word
DMOVH @R13+, @dir9	D	1D	2a	– – – –	(R13) → (dir9), R13 + = 2	Half word
DMOVB @dir8, R13	D	0A	b	– – – –	(dir8) → R13	Byte
DMOVB R13, @dir8	D	1A	a	– – – –	R13 → (dir8)	Byte
DMOVB @dir8, @R13+	D	0E	2a	– – – –	(dir8) → (R13), R13 + +	Byte
DMOVB @R13+, @dir8	D	1E	2a	– – – –	(R13) → (dir8), R13 + +	Byte

Note: The relations between the dir field of TYPE-D in the instruction format and the assembler description from disp8 to disp10 are as follows:

disp8 → dir + disp8
disp9 → dir = disp9>>1
disp10 → dir = disp10>>2
} Each disp is a code extension

- **Resource instructions (2 instructions)**

Mnemonic	Type	OP	Cycle	N Z V C	Operation	Remarks
LDRES @Ri+, #u4	C	BC	a	– – – –	(Ri) → u4 resource Ri + = 4	u4: Channel number
STRES #u4, @Ri+	C	BD	a	– – – –	u4 resource → (Ri) Ri + = 4	u4: Channel number

- **Co-processor instructions (4 instructions)**

Mnemonic	Type	OP	Cycle	N Z V C	Operation	Remarks
COPOP #u4, #CC, CRj, CRi	E	9F – C	2 + a	– – – –	Calculation	
COPLD #u4, #CC, Rj, CRi	E	9F – D	1 + 2a	– – – –	Rj → CRi	
COPST #u4, #CC, CRj, Ri	E	9F – E	1 + 2a	– – – –	CRj → Ri	
COPSV #u4, #CC, CRj, Ri	E	9F – F	1 + 2a	– – – –	CRj → Ri	No error traps

- **Other instructions (16 instructions)**

Mnemonic	Type	OP	Cycle	N Z V C	Operation	Remarks
NOP	E	9F – A	1	– – – –	No changes	
ANDCCR #u8 ORCCR #u8	D D	83 93	c c	C C C C C C C C	CCR and u8 → CCR CCR or u8 → CCR	
STILM #u8	D	87	1	– – – –	i8 → ILM	Set ILM immediate value
ADDSP #s10 *1	D	A3	1	– – – –	R15 + = s10	ADD SP instruction
EXTSB Ri EXTUB Ri EXTSH Ri EXTUH Ri	E E E E	97 – 8 97 – 9 97 – A 97 – B	1 1 1 1	– – – – – – – – – – – – – – – –	Sign extension 8 → 32 bits Zero extension 8 → 32 bits Sign extension 16 → 32 bits Zero extension 16 → 32 bits	
LDM0 (reglist) LDM1 (reglist) * LDM (reglist) *3	D D	8C 8D	*4 *4 –	– – – – – – – – – – – –	(R15) → reglist, R15 increment (R15) → reglist, R15 increment (R15 + +) → reglist,	Load-multi R0 to R7 Load-multi R8 to R15 Load-multi R0 to R15
STM0 (reglist) STM1 (reglist) * STM2 (reglist) *5	D D	8E 8F	*6 *6 –	– – – – – – – – – – – –	R15 decrement, reglist → (R15) R15 decrement, reglist → (R15) reglist → (R15 + +)	Store-multi R0 to R7 Store-multi R8 to R15 Store-multi R0 to R15
ENTER #u10 *2	D	0F	1+a	– – – –	R14 → (R15 – 4), R15 – 4 → R14, R15 – u10 → R15	Entrance processing of function
LEAVE	E	9F – 9	b	– – – –	R14 + 4 → R15, (R15 – 4) → R14	Exit processing of function
XCHB @Rj, Ri	A	8A	2a	– – – –	Ri → TEMP, (Rj) → Ri, TEMP → (Rj)	For SEMAFO management Byte data

*1: In the ADDSP instruction, the reference between u8 of TYPE-D in the instruction format and assembler description s10 is as follows.
s10 → s8 = s10>>2

*2: In the ENTER instruction, the reference between i8 of TYPE-C in the instruction format and assembler description u10 is as follows.
u10 → u8 = u10>>2

*3: If either of R0 to R7 is specified in reglist, assembler generates LDM0. If either of R8 to R15 is specified, assembler generates LDM1. Both LDM0 and LDM1 may be generated.

*4: The number of cycles needed for execution of LDM0 (reglist) and LDM1 (reglist) is given by the following calculation; $a \times (n - 1) + b + 1$ when “n” is number of registers specified.

*5: If either of R0 to R7 is specified in reglist, assembler generates STM0. If either of R8 to R15 is specified, assembler generates STM1. Both STM0 and STM1 may be generated.

*6: The number of cycles needed for execution of STM0 (reglist) and STM1 (reglist) is given by the following calculation; $a \times n + 1$ when “n” is number of registers specified.

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- **20-bit normal branch macro instructions**

Mnemonic		Operation	Remarks	
* CALL20	label20, Ri	Next instruction address → RP, label20 → PC	Ri: Temporary register	*1
* BRA20	label20, Ri	label20 → PC	Ri: Temporary register	*2
* BEQ20	label20, Ri	if (Z = = 1) then label20 → PC	Ri: Temporary register	*3
* BNE20	label20, Ri	ifs/Z = = 0	Ri: Temporary register	*3
* BC20	label20, Ri	ifs/C = = 1	Ri: Temporary register	*3
* BNC20	label20, Ri	ifs/C = = 0	Ri: Temporary register	*3
* BN20	label20, Ri	ifs/N = = 1	Ri: Temporary register	*3
* BP20	label20, Ri	ifs/N = = 0	Ri: Temporary register	*3
* BV20	label20, Ri	ifs/V = = 1	Ri: Temporary register	*3
* BNV20	label20, Ri	ifs/V = = 0	Ri: Temporary register	*3
* BLT20	label20, Ri	ifs/V xor N = = 1	Ri: Temporary register	*3
* BGE20	label20, Ri	ifs/V xor N = = 0	Ri: Temporary register	*3
* BLE20	label20, Ri	ifs/(V xor N) or Z = = 1	Ri: Temporary register	*3
* BGT20	label20, Ri	ifs/(V xor N) or Z = = 0	Ri: Temporary register	*3
* BLS20	label20, Ri	ifs/C or Z = = 1	Ri: Temporary register	*3
* BHI20	label20, Ri	ifs/C or Z = = 0	Ri: Temporary register	*3

*1: CALL20

(1) If label20 – PC – 2 is between –0x800 and +0x7fe, instruction is generated as follows;

```
CALL    label12
```

(2) If label20 – PC – 2 is outside of the range given in (1) or includes external reference symbol, instruction is generated as follows;

```
LDI:20  #label20, Ri
CALL    @Ri
```

*2: BRA20

(1) If label20 – PC – 2 is between –0x100 and +0xfe, instruction is generated as follows;

```
BRA     label9
```

(2) If label20 – PC – 2 is outside of the range given in (1) or includes external reference symbol, instruction is generated as follows;

```
LDI:20  #label20, Ri
JMP     @Ri
```

*3: Bcc20 (BEQ20 to BHI20)

(1) If label20 – PC – 2 is between –0x100 and +0xfe, instruction is generated as follows;

```
Bcc     label9
```

(2) If label20 – PC – 2 is outside of the range given in (1) or includes external reference symbol, instruction is generated as follows;

```
Bxcc    false        xcc is a revolt condition of cc
LDI:20  #label20, Ri
JMP     @Ri
false:
```

- **20-bit delayed branch macro instructions**

Mnemonic	Operation	Remarks
* CALL20:D label20, Ri	Next instruction address + 2 → RP, label20 → PC	Ri: Temporary register *1
* BRA20:D label20, Ri	label20 → PC	Ri: Temporary register *2
* BEQ20:D label20, Ri	if (Z = = 1) then label20 → PC	Ri: Temporary register *3
* BNE20:D label20, Ri	ifs/Z = = 0	Ri: Temporary register *3
* BC20:D label20, Ri	ifs/C = = 1	Ri: Temporary register *3
* BNC20:D label20, Ri	ifs/C = = 0	Ri: Temporary register *3
* BN20:D label20, Ri	ifs/N = = 1	Ri: Temporary register *3
* BP20:D label20, Ri	ifs/N = = 0	Ri: Temporary register *3
* BV20:D label20, Ri	ifs/V = = 1	Ri: Temporary register *3
* BNV20:D label20, Ri	ifs/V = = 0	Ri: Temporary register *3
* BLT20:D label20, Ri	ifs/V xor N = = 1	Ri: Temporary register *3
* BGE20:D label20, Ri	ifs/V xor N = = 0	Ri: Temporary register *3
* BLE20:D label20, Ri	ifs/(V xor N) or Z = = 1	Ri: Temporary register *3
* BGT20:D label20, Ri	ifs/(V xor N) or Z = = 0	Ri: Temporary register *3
* BLS20:D label20, Ri	ifs/C or Z = = 1	Ri: Temporary register *3
* BHI20:D label20, Ri	ifs/C or Z = = 0	Ri: Temporary register *3

*1: CALL20:D

(1) If label20 – PC – 2 is between –0x800 and +0x7fe, instruction is generated as follows;

```
CALL:D  label12
```

(2) If label20 – PC – 2 is outside of the range given in (1) or includes external reference symbol, instruction is generated as follows;

```
LDI:20  #label20, Ri
CALL:D  @Ri
```

*2: BRA20:D

(1) If label20 – PC – 2 is between –0x100 and +0xfe, instruction is generated as follows;

```
BRA:D   label9
```

(2) If label20 – PC – 2 is outside of the range given in (1) or includes external reference symbol, instruction is generated as follows;

```
LDI:20  #label20, Ri
JMP:D   @Ri
```

*3: Bcc20:D (BEQ20:D to BHI20:D)

(1) If label20 – PC – 2 is between –0x100 and +0xfe, instruction is generated as follows;

```
Bcc:D   label9
```

(2) If label20 – PC – 2 is outside of the range given in (1) or includes external reference symbol, instruction is generated as follows;

```
  Bxcc    false         xcc is a revolt condition of cc
  LDI:20  #label20, Ri
  JMP:D   @Ri
false:
```

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- **32-bit normal macro branch instructions**

Mnemonic		Operation	Remarks	
* CALL32	label32, Ri	Next instruction address → RP, label32 → PC	Ri: Temporary register	*1
* BRA32	label32, Ri	label32 → PC	Ri: Temporary register	*2
* BEQ32	label32, Ri	if (Z = = 1) then label32 → PC	Ri: Temporary register	*3
* BNE32	label32, Ri	ifs/Z = = 0	Ri: Temporary register	*3
* BC32	label32, Ri	ifs/C = = 1	Ri: Temporary register	*3
* BNC32	label32, Ri	ifs/C = = 0	Ri: Temporary register	*3
* BN32	label32, Ri	ifs/N = = 1	Ri: Temporary register	*3
* BP32	label32, Ri	ifs/N = = 0	Ri: Temporary register	*3
* BV32	label32, Ri	ifs/V = = 1	Ri: Temporary register	*3
* BNV32	label32, Ri	ifs/V = = 0	Ri: Temporary register	*3
* BLT32	label32, Ri	ifs/V xor N = = 1	Ri: Temporary register	*3
* BGE32	label32, Ri	ifs/V xor N = = 0	Ri: Temporary register	*3
* BLE32	label32, Ri	ifs/(V xor N) or Z = = 1	Ri: Temporary register	*3
* BGT32	label32, Ri	ifs/(V xor N) or Z = = 0	Ri: Temporary register	*3
* BLS32	label32, Ri	ifs/C or Z = = 1	Ri: Temporary register	*3
* BHI32	label32, Ri	ifs/C or Z = = 0	Ri: Temporary register	*3

*1: CALL32

(1) If label32 – PC – 2 is between –0x800 and +0x7fe, instruction is generated as follows;

```
CALL     label12
```

(2) If label32 – PC – 2 is outside of the range given in (1) or includes external reference symbol, instruction is generated as follows;

```
LDI:32   #label32, Ri
CALL     @Ri
```

*2: BRA32

(1) If label32 – PC – 2 is between –0x100 and +0xfe, instruction is generated as follows;

```
BRA      label9
```

(2) If label32 – PC – 2 is outside of the range given in (1) or includes external reference symbol, instruction is generated as follows;

```
LDI:32   #label32, Ri
JMP      @Ri
```

*3: Bcc32 (BEQ32 to BHI32)

(1) If label32 – PC – 2 is between –0x100 and +0xfe, instruction is generated as follows;

```
Bcc      label9
```

(2) If label32 – PC – 2 is outside of the range given in (1) or includes external reference symbol, instruction is generated as follows;

```
  Bxcc     false        xcc is a revolt condition of cc
  LDI:32   #label32, Ri
  JMP      @Ri
false:
```

- **32-bit delayed macro branch instructions**

Mnemonic	Operation	Remarks
* CALL32:D label32, Ri	Next instruction address + 2 → RP, label32 → PC	Ri: Temporary register *1
* BRA32:D label32, Ri	label32 → PC	Ri: Temporary register *2
* BEQ32:D label32, Ri	if (Z = = 1) then label32 → PC	Ri: Temporary register *3
* BNE32:D label32, Ri	ifs/Z = = 0	Ri: Temporary register *3
* BC32:D label32, Ri	ifs/C = = 1	Ri: Temporary register *3
* BNC32:D label32, Ri	ifs/C = = 0	Ri: Temporary register *3
* BN32:D label32, Ri	ifs/N = = 1	Ri: Temporary register *3
* BP32:D label32, Ri	ifs/N = = 0	Ri: Temporary register *3
* BV32:D label32, Ri	ifs/V = = 1	Ri: Temporary register *3
* BNV32:D label32, Ri	ifs/V = = 0	Ri: Temporary register *3
* BLT32:D label32, Ri	ifs/V xor N = = 1	Ri: Temporary register *3
* BGE32:D label32, Ri	ifs/V xor N = = 0	Ri: Temporary register *3
* BLE32:D label32, Ri	ifs/(V xor N) or Z = = 1	Ri: Temporary register *3
* BGT32:D label32, Ri	ifs/(V xor N) or Z = = 0	Ri: Temporary register *3
* BLS32:D label32, Ri	ifs/C or Z = = 1	Ri: Temporary register *3
* BHI32:D label32, Ri	ifs/C or Z = = 0	Ri: Temporary register *3

*1: CALL32:D

(1) If label32 – PC – 2 is between –0x800 and +0x7fe, instruction is generated as follows;

```
CALL:D   label12
```

(2) If label32 – PC – 2 is outside of the range given in (1) or includes external reference symbol, instruction is generated as follows;

```
LDI:32   #label32, Ri
CALL:D   @Ri
```

*2: BRA32:D

(1) If label32 – PC – 2 is between –0x100 and +0xfe, instruction is generated as follows;

```
BRA:D    label9
```

(2) If label32 – PC – 2 is outside of the range given in (1) or includes external reference symbol, instruction is generated as follows;

```
LDI:32   #label32, Ri
JMP:D    @Ri
```

*3: Bcc32:D (BEQ32:D to BHI32:D)

(1) If label32 – PC – 2 is between –0x100 and +0xfe, instruction is generated as follows;

```
Bcc:D    label9
```

(2) If label32 – PC – 2 is outside of the range given in (1) or includes external reference symbol, instruction is generated as follows;

```
  Bxcc     false        xcc is a revolt condition of cc
  LDI:32   #label32, Ri
  JMP:D    @Ri
false:
```

MB91101 Series

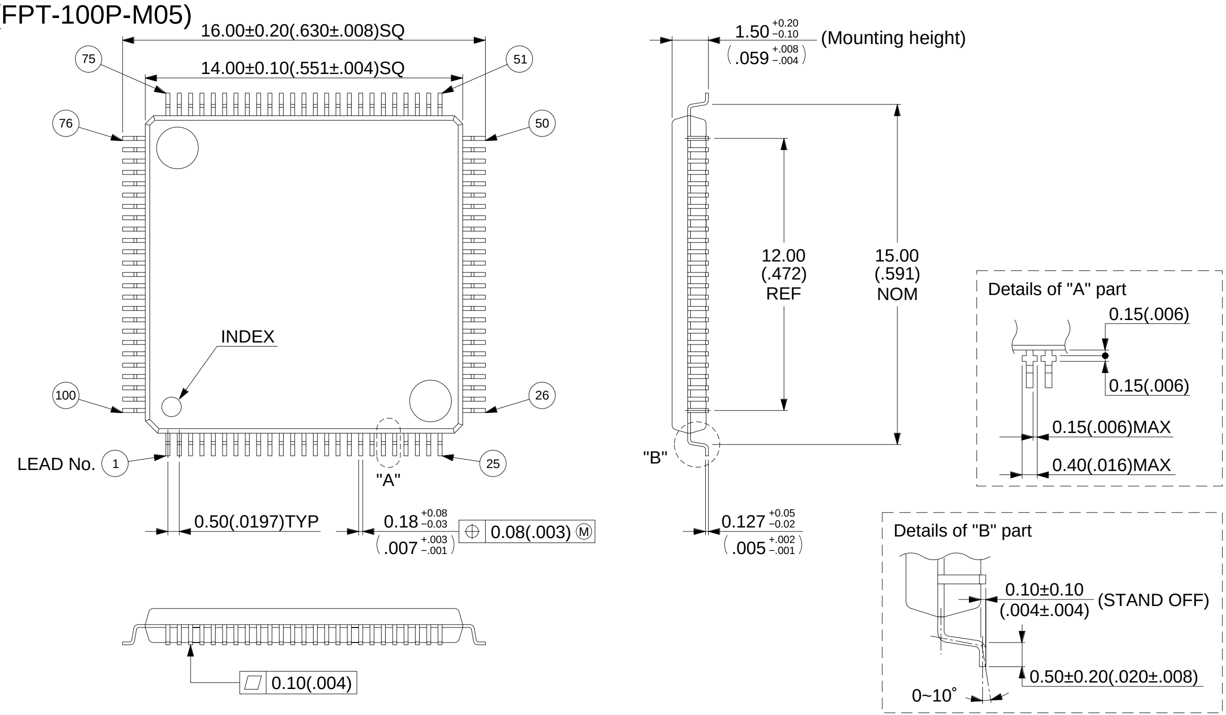
■ ORDERING INFORMATION

Part number	Package	Remarks
MB91101PFV-G-BND-R	100-pin Plastic LQFP (FPT-100P-M05)	
MB91101PF-G-BND-R	100-pin Plastic QFP (FPT-100P-M06)	

■ PACKAGE DIMENSIONS

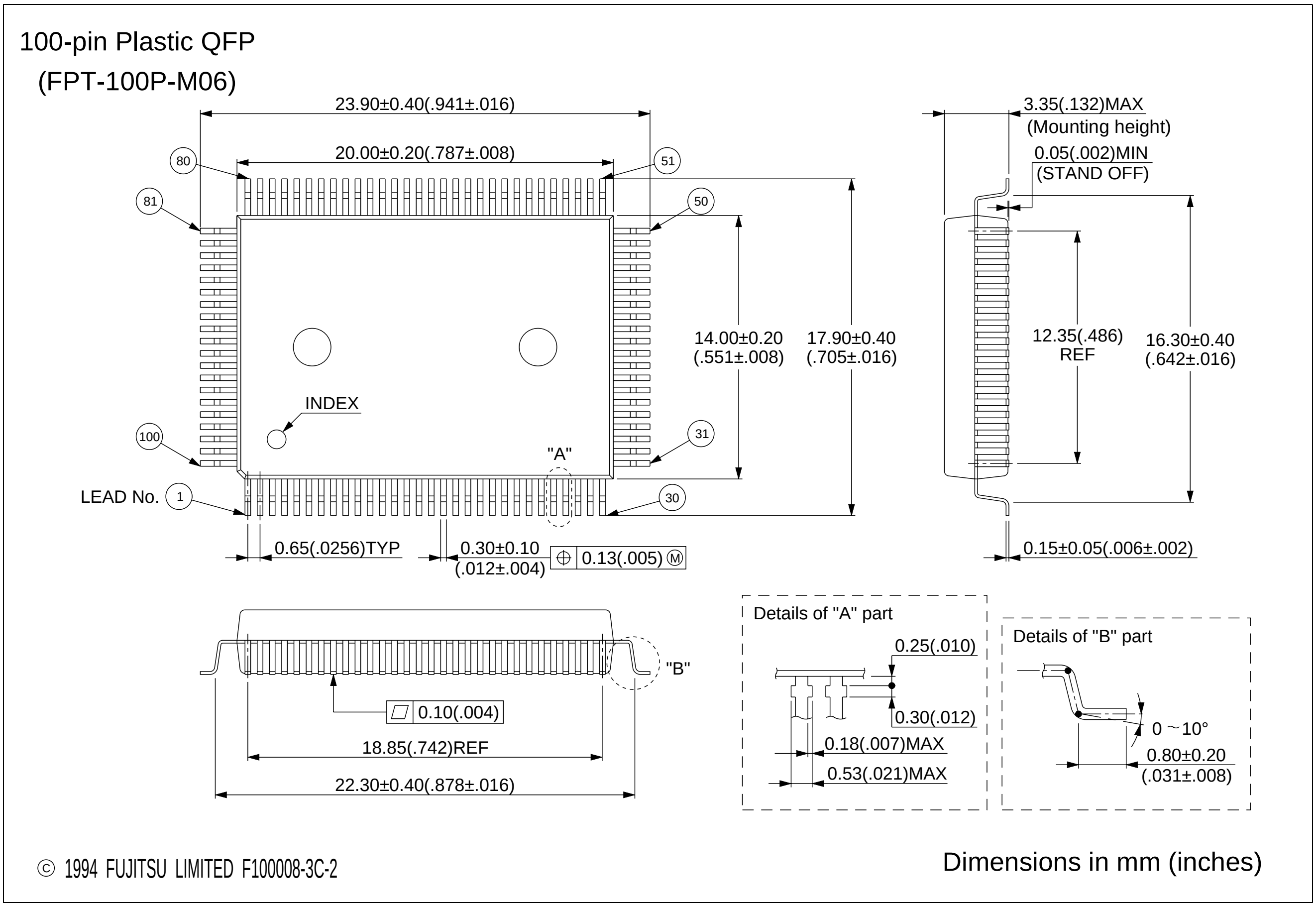
100-pin Plastic LQFP

(FPT-100P-M05)



Dimensions in mm (inches)

MB91101 Series



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